(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 566 219 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
17.07.2002 Bulletin 2002/29

(51) Int Cl.7: **H04N 11/04**, H04N 7/30

(21) Application number: **93201962.3**

(22) Date of filing: **22.04.1992**

(54) **Image processing apparatus**

Bildverarbeitungsgerät

Dispositif de traitement d'images

(84) Designated Contracting States:
DE ES FR GB IT NL

(30) Priority: **23.04.1991 JP 9228891**

(43) Date of publication of application:
20.10.1993 Bulletin 1993/42

(62) Document number(s) of the earlier application(s) in accordance with Art. 76 EPC:
92303572.9 / 0 510 921

(73) Proprietor: **CANON KABUSHIKI KAISHA**
Tokyo (JP)

(72) Inventor: **Fujii, Akio, c/o Canon Kabushiki Kaisha**
Ohta-ku, Tokyo (JP)

(74) Representative:
Beresford, Keith Denis Lewis et al
BERESFORD & Co.
2-5 Warwick Court,
High Holborn
London WC1R 5DH (GB)

(56) References cited:
EP-A- 0 239 076
EP-A- 0 323 363
EP-A- 0 400 756
EP-A- 0 401 854
EP-A- 0 469 648
EP-A- 0 475 251
EP-A- 0 481 768
EP-A- 0 510 929
WO-A-91/01613
DE-A- 4 034 535
US-A- 4 984 076

Printed by Jouve, 75001 PARIS (FR)

Description

[0001] The present invention relates to an image processing method and apparatus, and more particularly to an image processing method and apparatus for quantizing frequency conversion data and coding the quantized conversion data.

[0002] A number of color image compressing techniques have been proposed in the past. As a typical one of color still image coding techniques, there is proposed an adaptive discrete cosine transform coding method (hereinafter referred to as an ADCT method).

[0003] Fig. 3 is a conceptual view showing arrangement of an image coding apparatus using the ADCT method. It is assumed that an input image is given by data converted into 8 bits, i.e., 256 gradations, for each color in a not-shown analog-to-digital converter (hereinafter referred to as an A/D converter) and the number of colors is three, i.e., luminance Y, color P_B and color P_R, in this case.

[0004] The digital data of the luminance signal Y inputted through an input terminal 101 in Fig. 3 is subjected to two-dimensional discrete cosine transform (hereinafter abbreviated as DCT) in an N x N DCT circuit 102 in units of subblocks each comprising N x N pixels. Thereafter, the conversion coefficients are linearly quantized in a linear quantizer 113 with a quantizing step size being different for each of the conversion coefficients. The quantizing step sizes for respective conversion coefficients are given by values resulted from multiplying 2^S by quantization matrix elements of N x N in consideration of the fact that visual sensitivity for quantizing noise is different for each of the conversion coefficients. Here, S is 0 or a positive or negative integer and called a scaling factor. The image quality or the data to be generated is controlled depending on the value of S.

[0005] One example of the quantization matrix elements is shown in Fig. 5 in the case of 8 x 8. A quantization matrix generation circuit 111 is controlled by a control circuit 302 and generates a quantization matrix for the luminance signal Y. A switch 114 is changed over to select the side a for supplying the quantization matrix for the luminance signal Y to a multiplier 110. Using the scaling factor S supplied from a scaling factor generation circuit 301, the multiplier 110 multiplies 2^S by each quantized element of the quantization matrix. The multiplied results are supplied to the linear quantizer 103 where the conversion coefficients are linearly quantized by using the supplied results.

[0006] After the quantization, direct current conversion coefficients (hereinafter referred to as DC components) are supplied to a one-dimensional predictor 104 to calculate prediction values using several subblocks adjacent to each other, and prediction errors are subjected to Huffman coding in a Huffman encoder 105. More specifically, after dividing quantized outputs of the prediction errors into groups, the ID numbers of the groups to which the respective prediction errors belong are first subjected to Huffman coding, and which values in each group correspond to the respective prediction errors are then represented by using equi-length codes.

[0007] The conversion coefficients other than the above DC components, i.e., the alternating current conversion coefficients (hereinafter referred to as AC components), are supplied to a zigzag scan circuit 106 in which the AC components are scanned in a zigzag manner with two-dimensional frequencies from low-frequency component to high-frequency component as shown in Fig. 4, followed by Huffman coding in a Huffman encoder 107. More specifically, those conversion coefficients for which the quantized outputs are not 0 (hereinafter referred to as significant coefficients) are divided into groups depending on their values.

[0008] The ID numbers of the divided groups and the numbers of those conversion coefficients which are present between every two significant coefficients and for which the quantized outputs are 0 (hereinafter referred to as insignificant coefficients) are subjected in pair to Huffman coding. Subsequently, which values in each group correspond to the significant coefficients are represented by using equi-length codes.

[0009] Respective code strings of the DC components and the AC components are multiplexed in a multiplexer 108 and outputted from an output terminal 109.

[0010] Next, when the digital data of the chrominance signals P_B, P_R are inputted through the input terminal 101, the control circuit 302 controls the quantization matrix generation circuit 111 to generate quantization matrices for the chrominance signals P_B, P_R. The switch 114 is changed over to select the side b for supplying the quantization matrices for the chrominance signals to the multiplier 110. Subsequently, the chrominance signals processed in a like manner to the luminance signal Y as mentioned above for Huffman coding.

[0011] When the compression rate requires to be increased (for a higher degree of compression) from limitations in a transmission path or other reasons, control information is entered from a input terminal 303 so that the control circuit 302 controls a scaling factor generation circuit 301 to increase the scaling factor S. Conversely, in order to obtain a high-quality image, the scaling factor S is made smaller.

[0012] However, because the scaling factor S of the same value is used when coding the luminance signal Y and the chrominance signals P_B, P_R in the above prior art, there has accompanied a shortcoming that image quality in color areas (particularly in a red area to which human eyes are more sensitive) deteriorates to a remarkable extent, when the value of the scaling factor S is increased to obtain a high degree of compression.

[0013] The present invention is concerned with providing an image processing apparatus which can realize satis-

factory reproducibility of colors.

[0014] European Patent Application No. EP-A-0323363 discloses image processing apparatus in which quantizing and encoding are carried out in parallel on luminance and colour data.

[0015] Accordingly, in one aspect the present invention provides colour image coding apparatus as set out in claim 1.

[0016] From a second aspect the present invention comprises a colour image coding method as set out in claim 12.

[0017] In order that the present invention may be more readily understood, embodiments thereof will now be described by way of example and with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018]

Fig. 1 is a block diagram showing a first embodiment of the present invention;
Fig. 2 is a block diagram showing a second embodiment of the present invention;
Fig. 3 is a block diagram showing the prior art;
Fig. 4 is a diagram representing a zigzag scan;
Fig. 5 is a diagram showing one example of quantization matrix elements; and
Fig. 6 is a block diagram showing an application example of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0019] In the following embodiments of the present invention, a coefficient factor to be multiplied by quantization matrix elements for a chrominance signal is controlled depending on a scaling factor value S_0 of a luminance signal Y, thereby reducing an extent of deterioration in image quality even when the scaling factor value is increased for a higher compression rate.

[0020] Fig. 1 is a block diagram showing a first embodiment of the present invention. In the drawing, denoted by reference numeral 101 is an input terminal for digital image data, 102 is a DCT ciruit per N x N pixels, 103 is a linear quantizer for linearly quantizing conversion coefficients, 104 is a one-dimensional predictor for DC components, 105 is a. Huffman encoder, 106 is a zigzag scan circuit for scanning AC components in a zigzag pattern, 107 is a Huffman encoder, 108 is a multiplexer for multiplexing codes of the DC and AC components, and 109 is an output terminal. 110 is a multiplier for multiplying quantization matrix elements for luminance or chrominance by a scaling factor, 111 is a quantization matrix generation circuit for generating quantization matrices for luminance and chrominance, 112 is a control circuit for controlling the quantization matrix generation circuit and a scaling factor generation circuit, 113 is a scaling factor generation circuit for generating scaling factors or coefficients to be multiplied for a luminance signal Y and chrominance signals P_B, P_R, 114, 115 are select switches, and 116 is an input terminal through which control information (such as an amount of coded data) is entered to the control circuit.

[0021] Note that components having the same functions as those in Fig. 3 are denoted by the same reference numerals. The following description will be made about only different parts between the prior art and this embodiment.

[0022] The scaling factor generation circuit 113 is controlled by the control circuit 112 to generate the scaling factor value S_0 to be multiplied by the quantization matrix elements for the luminance signal Y and, at this time, the switch 115 is changed over to select the contact a. When conversion coefficients of the chrominance signal P_B are linearly quantized by the linear quantizer 103 after coding the luminance signal Y, the scaling factor generation circuit 113 is controlled by the control circuit 112 to generate a scaling factor S_B for P_B, and the switch 115 is changed over to select the contact b. In this case, S_B is generated as a function of S_0, for example, as expressed below:

$$S_B = f_B(S_0)$$

[0023] When conversion coefficients of the chrominance signal P_R are linearly quantized by the linear quantizer 103, the scaling factor generation circuit 113 is controlled by the control circuit 112 to generate a scaling factor S_R for P_R, and the switch 115 is changed over to select the contact c. In this case, S_R is generated as a function of S_0, for example, as expressed below:

$$S_R = f_R(S_0)$$

[0024] Example of function forms of S_B, S_R usable in this embodiment are enumerated below:

$$\text{i)} \quad S_B = f_B(S_0) = S_0 + XB,$$

$$S_R = f_R(S_0) = S_0 - XR$$

where XB, XR are positive constants

$$\text{ii)} \quad S_B = f_B(S_0) = \begin{cases} S_0 \times KB_1 & (S_0 \geq 0) \\ S_0 \times KB_2 & (S_0 < 0) \end{cases}$$

$$S_R = f_R(S_0) = \begin{cases} S_0 \times KR_1 & (S_0 \geq 0) \\ S_0 \times KR_2 & (S_0 < 0) \end{cases}$$

where KB_1, KB_2, KR_1, KR_2 are constants

$$\text{iii)} \quad S_B = f_B(S_0) = S_0 \times K_B(S_0),$$

$$S_R = f_R(S_0) = S_0 \times K_R(S_0)$$

where $K_B(S_0)$, $K_R(S_0)$ are functions of S_0

$$\text{iv)} \quad S_B = f_B(S_0) = S_0$$

$$S_R = f_R(S_0) = \begin{cases} S_0 & (S_0 < A) \\ C & (S_0 \geq A) \end{cases}$$

where C, A are constants

[0025] Optimum ones of the above functions and constants are selected depending on the compression rate required and the nature of an input image so that deterioration of image quality is minimized. This selection can be achieved by, for example, repeating the coding process several times with different quantization characteristics or performing the coding processes with different quantization characteristics in parallel as explained later.

[0026] As an alternative method of controlling respective quantization steps for the chrominance signals P_B, P_R, the coefficients to be multiplied by the quantization matrix elements for chrominance signals may be themseleves controlled rather than generating the scaling factors. In this case, the scaling factor generation circuit 113 generates coefficients M_B, M_R to be multiplied for the chrominance signals P_B, P_R in place of the scaling factors. M_B, M_R are functions of S_0 as expressed below:

$$M_B = g_B(S_0), \; M_R = g_R(S_0)$$

[0027] Example of function forms of M_B, M_R usable in this case are enumerated below:

$$\text{v)} \quad M_B = g_B(S_0) = 2^{S_0} + TB,$$

$$M_R = g_R(S_0) = 2^{S_0} - TR$$

where TB, TR are positive constants

$$\text{vi)}\quad M_B = g_B(S_0) = CB \times 2^{S_0},$$
$$M_R = g_R(S_0) = CR \times 2^{S_0}$$

where CB, CR are constants

$$\text{vii)}\quad M_B = g_B(s_0) = 2^{S_0} \times C_B(S_0),$$
$$M_R = g_R(S_0) = 2^{S_0} \times C_R(S_0),$$

where $C_B(S_0)$, $C_R(S_0)$ are functions of S_0

$$\text{viii)}\quad M_B = g_B(S_0) = 2^{S_0}$$
$$M_R = g_R(S_0) = \begin{cases} 2^{S_0} & (S_0 < B) \\ CO & (S_0 \geq B) \end{cases}$$

[0028] Optimum ones of the above functions and constants are selected depending on the compression rate required and the nature of an input image so that deterioration of image quality is minimized.

[0029] The compression rate can be changed by entering control information to the control circuit 112 through the input terminal 116 and changing the scaling factor value S_0. The mode for the method of deciding the quantizing steps for the chrominance signals P_B, P_R can also be changed by entering mode information to the control circuit 112 through the input terminal 116.

[0030] As mentioned above, since the scaling factor values of the luminance signal Y and the chrominance signals P_B, P_R are set by controlling the scaling factor values of the chrominance signals P_B, P_R depending on the scaling factor value S_0 of the luminance signal Y (such that in need of increasing the compression rate, a smaller scaling factor value is set for P_R which has higher visual sensitivity and a larger scaling factor value is set for P_B), an image with less deterioration in image quality can be obtained even when the compression rate is increased. Further, by controlling the coefficients to be multiplied by the quantization matrix elements for the chrominance signals using function such as f_B, f_R, g_B, g_R, the coding can be performed more efficiently than the case of setting those coefficients individually.

[0031] Moreover, even with the image data having other input form (such as GBR inputs) than the foregoing, the similar operating effect can also be achieved by weighing the coefficients to be multiplied by the quantization matrix elements in a like manner to the above case in match with the visual sensitivity of human eyes (e.g., such that in the case of GBR inputs, weighing is applied to the G input near a luminance signal, the B input and the R input in this order).

(Another Embodiment)

[0032] Fig. 2 shows a second embodiment of the present invention. Components having the same functions as those in the prior art are denoted by the same reference numerals and will not be described here. Blocks a, b and c circumscribed by broken lines all function in a like manner. However, an input to the block a is only the luminance signal Y, an input to the block b is only the chrominance signal P_B, and an input to the block c is only the chrominance signal P_C. Thus, the luminance signal and the chrominance signals are separately processed in parallel for coding. Accordingly, a control circuit 222 supplies a control signal suitable for parallel processing to a quantization matrix generation circuit 221 so that the quantization matrices for the luminance signal and the chrominance signals are generated almost at the same timing. Likewise, a scaling factor generation circuit 220 is controlled by the control circuit 222 to generate scaling factors S_Y, S_B, S_R for the luminance signal Y and the chrominance signals P_B, P_R almost at the same timing. S_Y, S_B, S_R are functions of S_0 as expressed below:

$$S_Y = S_0,\ S_B = f_B(S_0),\ S_R = f_R(S_0)$$

[0033] Alternatively, the scaling factor generation circuit 220 may generate coefficients to be directly multiplied by the quantization matrix elements for the chrominance signals. In this case, coefficients M_B, M_R used for the chrominance

signals M_B, M_R are given by:

$$M_B = g_B(S_0),\ M_R = g_R(S_0)$$

[0034] By so arranging, it is possible to not only obtain an image with less deterioration in image quality even at the increased compression rate, but also adapt to high-speed coding through parallel processing, which permits real-time coding of moving images and the like.

[0035] As explained above, by setting the scaling factor values or the coefficients themselves to be multiplied by the quantization matrix elements for the luminance signal Y and the chrominance signals P_B, P_R separately, and controlling the scaling factor values or the coefficients themselves to be multiplied by the quantization matrix elements for the chrominance signals P_B, P_R depending on the scaling factor value S_0 of the luminance signal Y, there can be obtained an image with less deterioration in image quality corresponding to the compression rate (namely, an image with less deterioration in quality of color images can be obtained even at the increased compression rate through such a control, for example, that in need of increasing the compression rate, a smaller scaling factor value than that of the luminance signal Y is set for the chrominance P_R which has higher visual sensitivity and a larger scaling factor value is set for the chrominance signal P_B). Further, by controlling the coefficients to be multiplied by the quantization matrix elements for the chrominance signals using functions, the coding can be performed more efficiently than the case of setting those coefficients individually.

[0036] Thus, according to the present invention, it is possible to provide an image encoding apparatus and method with which a reproduced image of high quality can be obtained.

[0037] An example of the present invention applied to a moving image encoding apparatus will be described below in detail. Fig. 6 is a block diagram of the apparatus.

[0038] In the drawing, denoted by 20 is an input terminal for an analog TV signal. The TV signal sensed by using a CCD sensor and inputted through the terminal 20 is converted by an A/D converter 22 into a digital signal of 8 bits. The digital signal is divided into blocks each comprising (8 x 8) pixels by an (8 x 8) block formation circuit 26 which operates in a like manner to the (N x N) DCT circuit 102 in Fig. 1, the blocks being supplied to a DCT circuit 28 one by one.

[0039] Pixel data D_{11} to D_{88} of each block are converted by the DCT circuit 28 into a data matrix X_{11} to X_{88} for two-dimensional frequency regions as with the case of Fig. 1, followed by being supplied to quantization circuits 32a to 32d and a 1F (one-frame) delay circuit 34.

[0040] A quantization matrix generation circuit 36 generates similar matrices to those generated from the aforesaid quantization matrix generation circuit 111.

[0041] Supplied to multipliers 38a to 38d are initial coefficients C_1 to C_4 as control coefficients (scaling factors) C from a coefficient calculator 48. As with the case of Fig. 1, the multipliers 38a to 38d multiply outputs of the quantization matrix generation circuit 36 and the control coefficients C_X for respective components, i.e., (W_{ij} x C_X/C_0), the multiplied results being outputted to the quantization circuits 32a to 32d. The quantization circuits 32a to 32d respectively quantize conversion coefficients with the quantizing steps controlled by the control coefficients C_1 to C_4 and output the quantized values to VLCs (Variable Length Coders) 40a to 40d.

[0042] In this embodiment, the VLCs 40a to 40d do not output the actual coded data, but output only information nb1 to nb4 of total bit number for each image as resulted from the similar processing to an ordinary VLC.

[0043] Using the information nb1 to nb4 outputted- from the VLCs 40a to 40d and the control coefficients C_1 to C_4, the coefficient calculator 48 calculates a control coefficient C_5 desired for the total bit number and outputs it to a multiplier 38e.

[0044] The coefficient calculator 48 also outputs control coefficients C_6, C_7 as an approximate value of C_5 to multipliers 38f, 38g and, on the other hand, outputs the control coefficients C_5 to C_7 to terminals 44a to 44c, respectively.

[0045] It is here assumed that when $C_n \leqq C_5 \leqq C_{n+1}$ holds for C_5, C_6 and C_7 meet the relationships $C_n \leqq C_6 < C_5$ and $C_5 < C_7 \leqq C_{n+1}$, respectively, and n meets the relationship $1 \leqq n \leqq 3$.

[0046] The multipliers 38e to 38g respectively multiply outputs of the quantization matrix generation circuit 36 and the control coefficients C_5 to C_7 as with the multipliers 38a to 38d, the multiplied results being outputted to quantization circuits 32e to 32g within a vertical blanking period.

[0047] Meanwhile, those DCT conversion coefficients resulted from delaying DCT conversion coefficients through one frame by the 1F delay circuit 34 are inputted to the quantization circuits 32e to 32g.

[0048] The conversion coefficients are quantized in the quantization circuits 32e to 32g with the quantizing steps controlled by the control coefficients C_5 to C_7, and the quantized values are outputted to VLCs 40e to 40g. In this embodiment, the VLCs 40e to 40g output the actual coded data to entry buffers 42a to 42c and also output the total bit numbers nb5 to nb7 to a judgment circuit 50. The judgment circuit 50 delivers such an output to switches 44 and 46 as to select the quantization result which is less than the desired total bit number and nearest thereto. The entry buffers 42a to 42c store the coded data until the judgment circuit 50 issues the judgment result. The switch 44 selects

one of the control coefficients in accordance with the judgment result and outputs it to a multiplexer 52. Also, the switch 46 selects one of the coded data and outputs it to the multiplexer 52. The multiplexer 52 multiplexes the control coefficient and the coded data, followed by outputting to an output terminal 54.

[0049] The scaling factor for quantizing the chrominance data may be controlled independently rather than being dependent on the scaling factor for quantizing the luminance data as stated before. In other words, the luminance data and the chrominance data may be coded in a completely parallel manner.

[0050] The scaling factor may be fixed in one frame of an image as mentioned before, or may be varied per block of N x N pixels.

[0051] Further, the scaling factor may be controlled depending on the amount of coded data resulted from the coding, or may be controlled depending on whether the original image is a line image including characters and the like or a natural image.

[0052] Additionally, while the component Y is extracted as luminance data and the components P_B, P_R are extracted as chrominance data in the above embodiments, those components may be (Y, C_R, C_B), (L*, a*, b*), (L*, u*, v*), (Y, u, v) or the like.

[0053] Moreover, the functions of the control circuit 112, the scaling factor generation circuit 113 and the quantization matrix generation circuit 111 can be executed by a CPU and a RAM, a ROM, etc. connected to the CPU.

[0054] It should be understood that the present invention is not limited to the embodiments as set forth above and may be variously changed and modified within the scope of the invention defined in the attached claims.

Claims

1. A colour image coding apparatus comprising:

   input means (20) for inputting image data representing a colour image and including luminance and chrominance data;
   quantizing means (32e-32g) for quantizing the image data; and
   encoding means (40e-40g) for encoding the quantized image data,

   characterized in that
   said quantizing means includes a first quantizer (32e) for quantizing the image data by using a first quantizing parameter and a second quantizer (32g) for quantizing the same image data by using a second quantizing parameter different from the first quantizing parameter each of said first and second quantizing being operative to quantize said luminance data and chrominance data,
   said encoding means includes a first encoder (40g) for encoding the image data quantized by said first quantizer and a second encoder (40e) for encoding the image data quantized by said second quantizer, and
   said first and second quantizers quantize the same image data in parallel and said first and second encoders perform encoding operations in parallel.

2. Apparatus according to claim 1 and further comprising means (50) for selecting between the outputs of said first and second encoders so as to select for output the quantization result which is both less than and nearest to a desired data amount.

3. Apparatus according to claim 1 or claim 2, including means for selecting quantizing parameters by evaluating a corresponding parameter which relates to the contents of the colour image.

4. Apparatus according to any preceding claim, further comprising means (48) for generating said first and second quantizing parameters.

5. Apparatus according to any one of the preceding claims, further comprising evaluating means for evaluating amounts of encoded image data to be output from said first and second encoding means.

6. Apparatus according to claim 3, wherein said evaluating means include:

   first and second initial quantizers (32a-32d);
   a quantization matrix generation circuit (36) adapted to generate initial control coefficients for said initial quantizers;
   first and second initial encoding means associated with the outputs of said first and second initial quantizers

and adapted to supply bit number information to a coefficient calculator (48) adapted to calculate control coefficients for said first and second quantizers.

7. Apparatus according to any one of the preceding claims, further comprising converting means (28) for converting said image data into spatial frequency components and wherein the output of said converting means is supplied to said first and second quantizers.

8. Apparatus according to any one of the preceding claims, further comprising generating means (36) for generating a quantizing matrix for said first and second quantizers.

9. Apparatus according to any one of the preceding claims, wherein said encoders are adapted to perform variable-length coding.

10. Apparatus according to any one of the preceding claims, wherein said input means comprise a CCD sensor.

11. Apparatus according to any one of the preceding claims and adapted to encode a moving colour image.

12. A method of encoding a colour image comprising:

inputting image data representing a colour image and including luminance and chrominance data;
quantizing the image data; and
encoding the quantized image data,

characterized in that
the quantizing step includes quantizing the image data by utilising a first quantizer which uses a first quantizing parameter and quantizing in parallel the same image data by utilising a second quantizer which uses a second quantizing parameter different from the first quantizing parameter, each of said first and second quantizer quantizing said luminance and said chrominance data, and
encoding in parallel the image data quantized using said first quantizing parameter and the image data quantized using said second quantizing parameter.

13. A method according to claim 12 and including selecting (50) between the encoded first and second image data which has been encoded in parallel so as to select for output the quantization result which is both less than and nearest to a desired data amount.

14. A method according to claim 12 or 13, further comprising the step of generating (48) said first and second quantizing parameters.

15. A method according to any one of claims 12, 13 or 14, and including selecting quantizing parameters by evaluating a corresponding parameter which relates to the contents of the colour image.

16. A method according to any one of claims 12 to 15 comprising:

converting said image data into spatial frequency components and supplying the spatial frequency components for quantization using said first and second quantizing parameters via a delay circuit.

17. A method according to any one of claims 12 to 16, wherein encoding is carried out by variable-length encoders.

18. A method according to any one of claims 12 to 17, comprising inputting the image data representing a colour image by means of a CCD sensor.

19. A method according to any one of claims 12 to 18, wherein the input image data represents a moving colour image.

Patentansprüche

1. Farbbildkodiergerät mit
einer Eingabeeinrichtung (20) zur Eingabe von Bilddaten, die ein Farbbild darstellen und Luminanz- und

Chrominanzdaten enthalten,

einer Quantisiereinrichtung (32e-32g) zur Quantisierung der Bilddaten und

einer Kodiereinrichtung (40e-40g) zur Kodierung der quantisierten Bilddaten,

dadurch gekennzeichnet, dass

die Quantisiereinrichtung einen ersten Quantisierer (32e) zur Quantisierung der Bilddaten unter Verwendung eines ersten Quantisierungsparameters und einen zweiten Quantisierer (32g) zur Quantisierung der gleichen Bilddaten unter Verwendung eines zweiten Quantisierungsparameters enthält, der von dem ersten Quantisierungsparameter verschieden ist, wobei der erste und der zweite Quantisierer beide zur Quantisierung der Luminanzdaten und Chrominanzdaten eingerichtet sind,

die Kodiereinrichtung einen ersten Kodierer (40g) zur Kodierung der durch den ersten Quantisierer quantisierten Bilddaten und einen zweiten Kodierer (40e) zur Kodierung der durch den zweiten Quantisierer quantisierten Bilddaten enthält, und

der erste und der zweite Quantisierer die gleichen Bilddaten parallel quantisieren und der erste und der zweite Kodierer die Kodiervorgänge parallel durchführen.

2. Gerät nach Anspruch 1, ferner mit einer Einrichtung (50) zur Auswahl zwischen den Ausgaben des ersten und zweiten Kodierers zur Auswahl der Ausgabe des Quantisierungsergebnisses, das sowohl geringer als eine gewünschte Datenmenge als auch dieser am nächsten ist.

3. Gerät nach Anspruch 1 oder 2, mit einer Einrichtung zur Auswahl von Quantisierungsparametern durch Auswertung eines entsprechenden Parameters, der sich auf die Inhalte des Farbbildes bezieht.

4. Gerät nach einem der vorhergehenden Ansprüche, ferner mit einer Einrichtung (48) zur Erzeugung des ersten und zweiten Quantisierungsparameters.

5. Gerät nach einem der vorhergehenden Ansprüche, ferner mit einer Auswerteeinrichtung zur Auswertung von Mengen kodierter Bilddaten, die aus der ersten und zweiten Kodiereinrichtung auszugeben sind.

6. Gerät nach Anspruch 3, wobei die Auswerteeinrichtung enthält:

erste und zweite Anfangsquantisierer (32a-32d),

eine Quantisierungsmatrix-Erzeugungsschaltung (36) zur Erzeugung von Anfangssteuerkoeffizienten für die Anfangsquantisierer, und

erste und zweite Anfangskodiereinrichtungen, die mit den Ausgaben der ersten und zweiten Anfangsquantisierer assoziiert sind und zur Zufuhr von Bitzahlinformationen zu einer Koeffizientenberechnungseinrichtung (48) zur Berechnung von Steuerkoeffizienten für den ersten und zweiten Quantisierer eingerichtet sind.

7. Gerät nach einem der vorhergehenden Ansprüche, ferner mit einer Umwandlungseinrichtung (28) zur Umwandlung der Bilddaten in Ortsfrequenzkomponenten, wobei die Ausgabe der Umwandlungseinrichtung dem ersten und zweiten Quantisierer zugeführt wird.

8. Gerät nach einem der vorhergehenden Ansprüche, ferner mit einer Erzeugungseinrichtung (36) zur Erzeugung einer Quantisierungsmatrix für den ersten und zweiten Quantisierer.

9. Gerät nach einem der vorhergehenden Ansprüche, wobei die Kodierer zur Durchführung einer variablen Längenkodierung eingerichtet sind.

10. Gerät nach einem der vorhergehenden Ansprüche, wobei die Eingabeeinrichtung einen CCD-Sensor umfasst.

11. Gerät nach einem der vorhergehenden Ansprüche, das zur Kodierung eines bewegten Farbbildes eingerichtet ist.

12. Verfahren zur Kodierung eines Farbbildes, mit den Schritten

Eingeben von Bilddaten, die ein Farbbild darstellen und Luminanz- und Chrominanzdaten enthalten,

Quantisieren der Bilddaten und

Kodieren der quantisierten Bilddaten,

dadurch gekennzeichnet, dass

der Quantisierungsschritt eine Quantisierung der Bilddaten unter Verwendung eines ersten Quantisierers, der einen ersten Quantisierungsparameter verwendet, und eine parallele Quantisierung der gleichen Bilddaten

unter Verwendung eines zweiten Quantisierers enthält, der einen zweiten Quantisierungsparameter verwendet, der von dem ersten Quantisierungsparameter verschieden ist, wobei der erste und der zweite Quantisierer beide die Luminanz- und die Chrominanzdaten quantisieren, und **gekennzeichnet durch** den Schritt

paralleles Kodieren der unter Verwendung des ersten Quantisierungsparameters quantisierten Bilddaten und der unter Verwendung des zweiten Quantisierungsparameters quantisierten Bilddaten.

13. Verfahren nach Anspruch 12, mit der Auswahl (50) zwischen den kodierten ersten und zweiten Bilddaten, die parallel kodiert wurden, zur Auswahl der Ausgabe des Quantisierungsergebnisses, das sowohl geringer als eine gewünschte Datenmenge als auch dieser am nächsten ist.

14. Verfahren nach Anspruch 12 oder 13, ferner mit dem Schritt der Erzeugung (48) des ersten und zweiten Quantisierungsparameters.

15. Verfahren nach einem der Ansprüche 12 bis 14, mit der Auswahl von Quantisierungsparametern durch Auswertung eines entsprechenden Parameters, der sich auf die Inhalte des Farbbildes bezieht.

16. Verfahren nach einem der Ansprüche 12 bis 15, mit dem Schritt

Umwandeln der Bilddaten in Ortsfrequenzkomponenten und Zuführen der Ortsfrequenzkomponenten zur Quantisierung unter Verwendung des ersten und zweiten Quantisierungsparameters über eine Verzögerungsschaltung.

17. Verfahren nach einem der Ansprüche 12 bis 16, wobei das Kodieren durch variable Längenkodierer ausgeführt wird.

18. Verfahren nach einem der Ansprüche 12 bis 17, mit der Eingabe der ein Farbbild darstellenden Bilddaten mittels eines CCD-Sensors.

19. Verfahren nach einem der Ansprüche 12 bis 18,wobei die eingegebenen Bilddaten ein bewegtes Farbbild darstellen.

Revendications

1. Appareil de codage d'images en couleurs, comportant :

un moyen d'entrée (20) destiné à l'entrée de données d'image représentant une image en couleurs et comprenant des données de luminance et de chrominance ;
un moyen de quantification (32e-32g) destiné à quantifier les données d'image ; et
un moyen de codage (40e-40g) destiné à coder les données d'image quantifiées, **caractérisé en ce que**
ledit moyen de quantification comprend un premier quantificateur (32e) destiné à quantifier les données d'image en utilisant un premier paramètre de quantification et un second quantificateur (32g) destiné à quantifier les mêmes données d'image en utilisant un second paramètre de quantification différent du premier paramètre de quantification, chacune desdites première et seconde quantifications ayant pour effet de quantifier lesdites données de luminance et lesdites données de chrominance ;
ledit moyen de codage comprenant un premier codeur (40g) destiné à coder les données d'image quantifiées par ledit premier quantificateur et un second codeur (40e) destiné à coder les données d'image quantifiées par ledit second quantificateur, et
lesdits premier et second quantificateurs quantifient les mêmes données d'image en parallèle et lesdits premier et second codeurs effectuent des opérations de codage en parallèle.

2. Appareil selon la revendication 1 et comportant en outre un moyen (50) destiné à sélectionner entre les signaux de sortie desdits premier et second codeurs afin de sélectionner pour la sortie le résultat de la quantification qui est à la fois en dessous et le plus proche d'une quantité de données souhaitée.

3. Appareil selon la revendication 1 ou la revendication 2, comprenant un moyen pour sélectionner des paramètres de quantification en évaluant un paramètre correspondant qui se rapporte au contenu de l'image en couleurs.

4. Appareil selon l'une quelconque des revendications précédentes, comprenant en outre un moyen (48) destiné à

générer lesdits premier et second paramètres de quantification.

5. Appareil selon l'une quelconque des revendications précédentes, comportant en outre des moyens d'évaluation destinés à évaluer des quantités de données d'image codées devant être délivrées en sortie desdits premier et second moyens de codage.

6. Appareil selon la revendication 3, dans lequel lesdits moyens d'évaluation comprennent :

   des premier et second quantificateurs initiaux (32a-32d) ;
   un circuit (36) de génération de matrice de quantification conçu pour générer des coefficients de commande initiale pour lesdits quantificateurs initiaux ;
   des premier et second moyens de codage initial associés aux sorties desdits premier et second quantificateurs initiaux et conçus pour fournir une information de nombres de bits à un calculateur (48) de coefficients conçu pour calculer des coefficients de commande pour lesdits premier et second quantificateurs.

7. Appareil selon l'une quelconque des revendications précédentes, comportant en outre un moyen de conversion (28) destiné à convertir lesdites données d'image en composantes de fréquence spatiale et dans lequel le signal de sortie dudit moyen de conversion est appliqué auxdits premier et second quantificateurs.

8. Appareil selon l'une quelconque des revendications précédentes, comportant en outre un moyen de génération (36) destiné à générer une matrice de quantification pour lesdits premier et second quantificateurs.

9. Appareil selon l'une quelconque des revendications précédentes, dans lequel lesdits codeurs sont conçus pour effectuer un codage de longueur variable.

10. Appareil selon l'une quelconque des revendications précédentes, dans lequel lesdits moyens d'entrée comprennent un capteur CCD.

11. Appareil selon l'une quelconque des revendications précédentes et conçu pour coder une image cinématographique en couleurs.

12. Procédé de codage d'une image en couleurs comprenant :

   l'entrée de données d'image représentant une image en couleurs et comprenant des données de luminance et de chrominance ;
   la quantification des données d'image ; et
   le codage des données d'image quantifiées,

   caractérisé en ce que
   l'étape de quantification comprend la quantification des données d'image en utilisant un premier quantificateur qui utilise un premier paramètre de quantification et la quantification en parallèle des mêmes données d'image en utilisant un second quantificateur qui utilise un second paramètre de quantification différent du premier paramètre de quantification, chacun desdits premier et second quantificateurs quantifiant lesdites données de luminance et de chrominance, et
   le codage en parallèle des données d'image quantifiées en utilisant ledit premier paramètre de quantification et des données d'image quantifiées en utilisant ledit second paramètre de quantification.

13. Procédé selon la revendication 12 et comprenant une sélection (50) entre les premières et secondes données d'image codées qui ont été codées en parallèle afin de sélectionner pour la sortie le résultat de la quantification qui est à la fois en dessous et le plus proche d'une quantité de données souhaitée.

14. Procédé selon la revendication 12 ou 13, comprenant en outre l'étape de génération (48) desdits premier et second paramètres de quantification.

15. Procédé selon l'une quelconque des revendications 12, 13 ou 14, et comprenant la sélection de paramètres de quantification en évaluant un paramètre correspondant qui se rapporte au contenu de l'image en couleurs.

16. Procédé selon l'une quelconque des revendications 12 à 15, comprenant :

la conversion desdites données d'image en composantes de fréquence spatiale et la fourniture des composantes de fréquence spatiale pour une quantification en utilisant lesdits premier et second paramètres de quantification par l'intermédiaire d'un circuit à retard.

17. Procédé selon l'une quelconque des revendications 12 à 16, dans lequel un codage est effectué par des codeurs de longueur variable.

18. Procédé selon l'une quelconque des revendications 12 à 17, comprenant l'entrée des données d'image représentant une image en couleurs au moyen d'un capteur CCD.

19. Procédé selon l'une quelconque des revendications 12 à 18, dans lequel les données d'image d'entrée représentent une image cinématographique en couleurs.

FIG.1

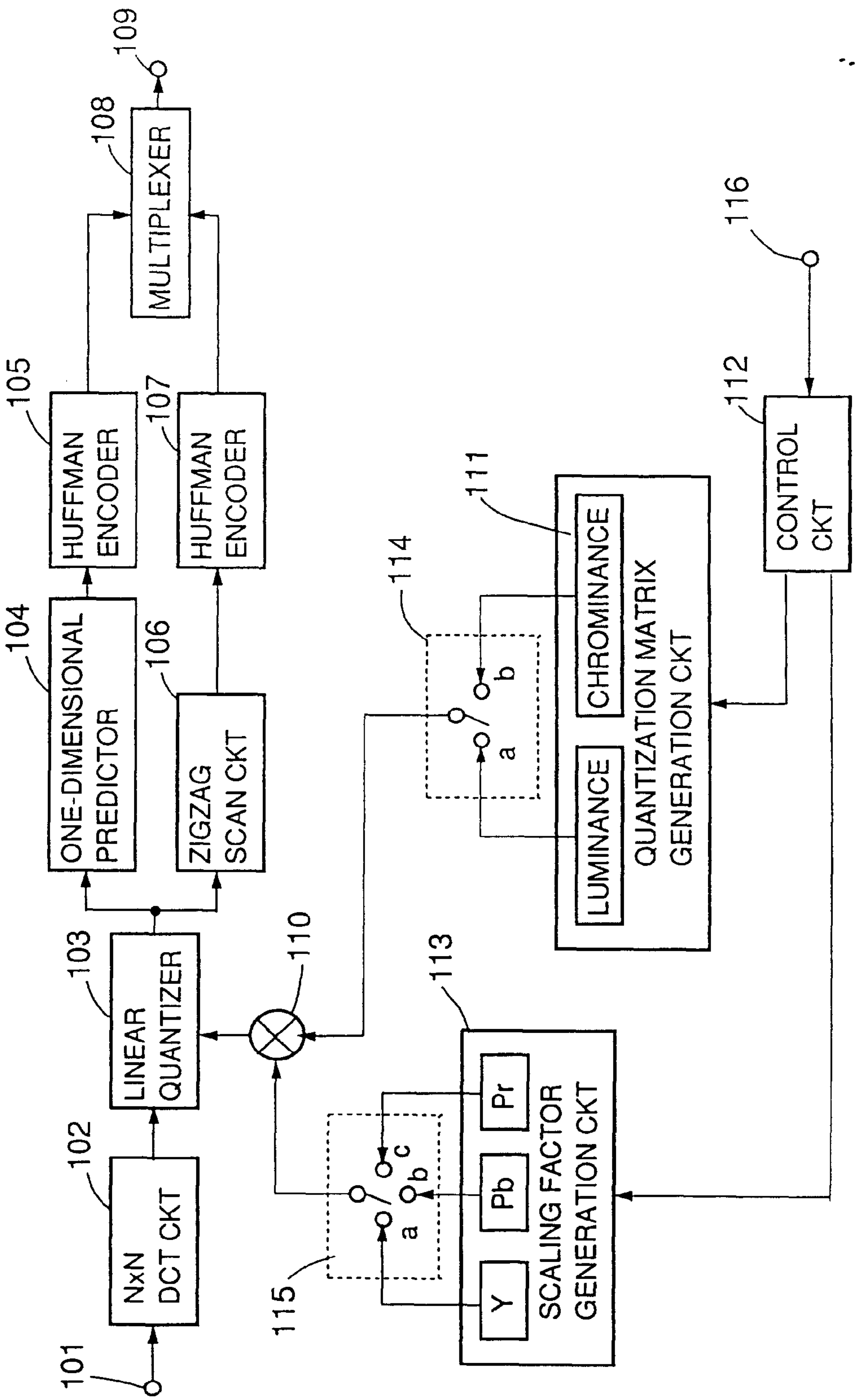
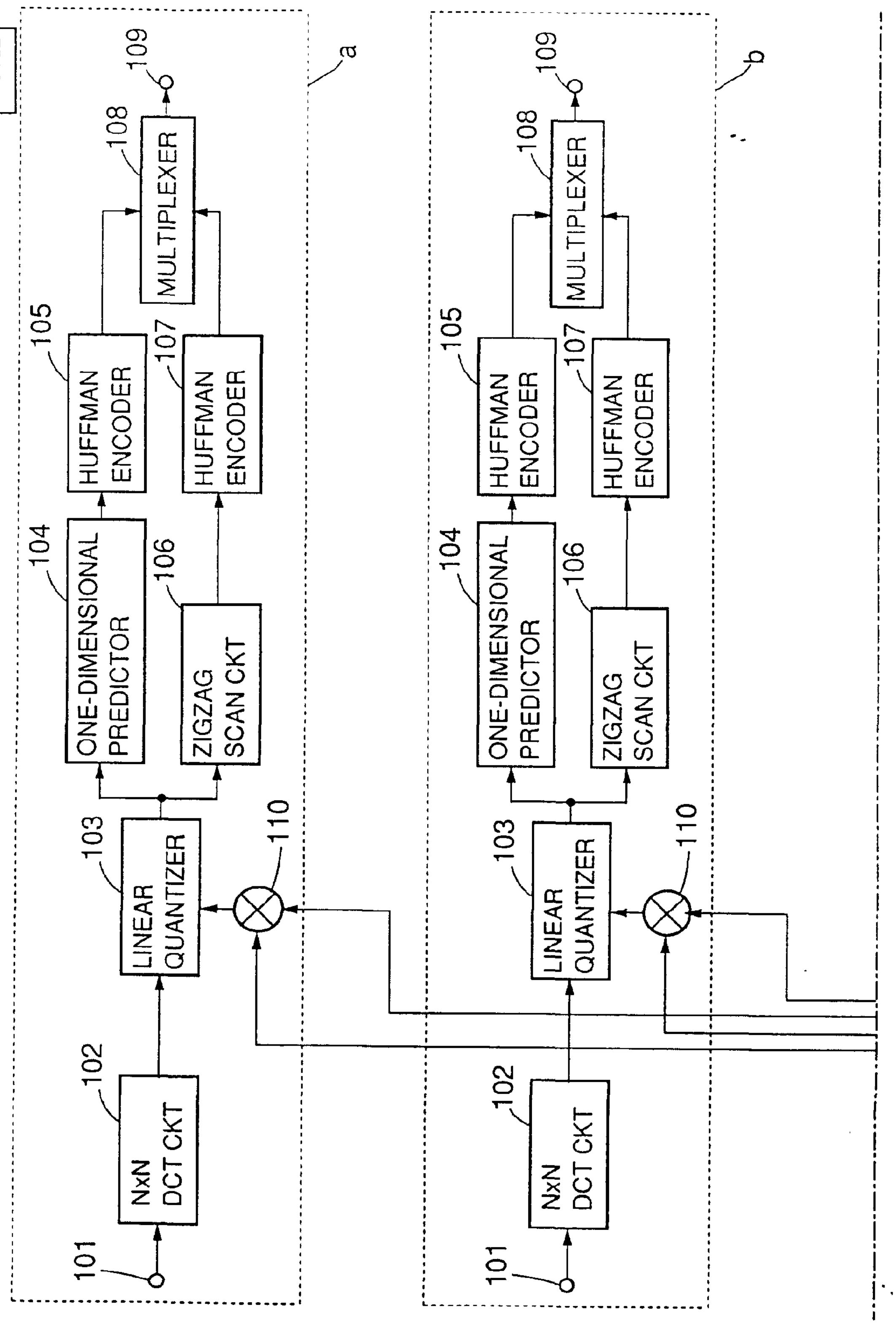

101
NxN DCT CKT
102
LINEAR QUANTIZER
103
ONE-DIMENSIONAL PREDICTOR
104
HUFFMAN ENCODER
105
ZIGZAG SCAN CKT
106
HUFFMAN ENCODER
107
MULTIPLEXER
108
109
110
CHROMINANCE
LUMINANCE
QUANTIZATION MATRIX GENERATION CKT
111
CONTROL CKT
112
Y
Pb
Pr
SCALING FACTOR GENERATION CKT
113
a
b
114
a
b
c
115
116

FIG.2A

FIG.2A | FIG.2B



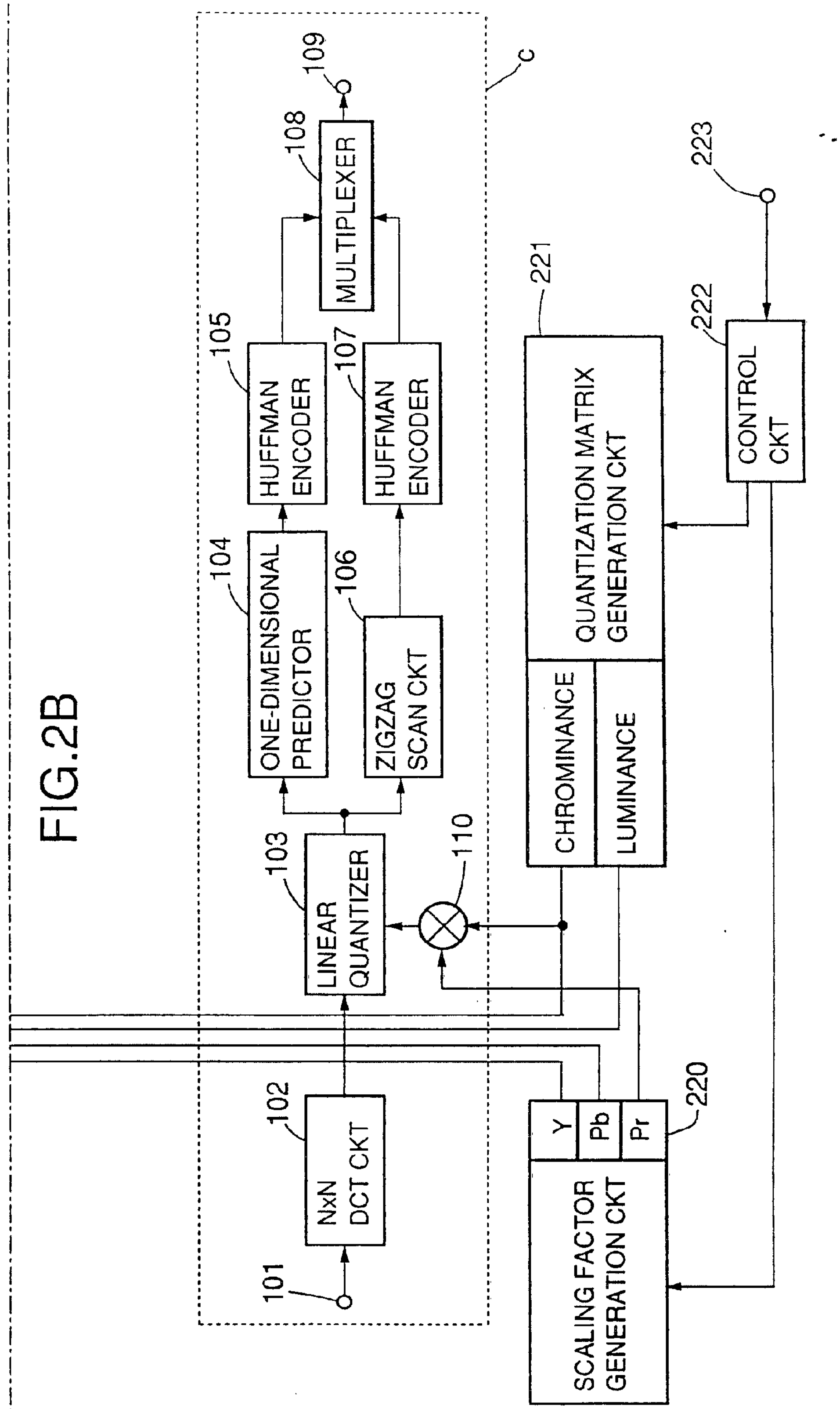

101
NxN DCT CKT
102
LINEAR QUANTIZER
103
ONE-DIMENSIONAL PREDICTOR
104
HUFFMAN ENCODER
105
ZIGZAG SCAN CKT
106
HUFFMAN ENCODER
107
MULTIPLEXER
108
109
110
C
SCALING FACTOR GENERATION CKT
Y
Pb
Pr
220
CHROMINANCE
LUMINANCE
QUANTIZATION MATRIX GENERATION CKT
221
CONTROL CKT
222
223

FIG.2B

FIG.3

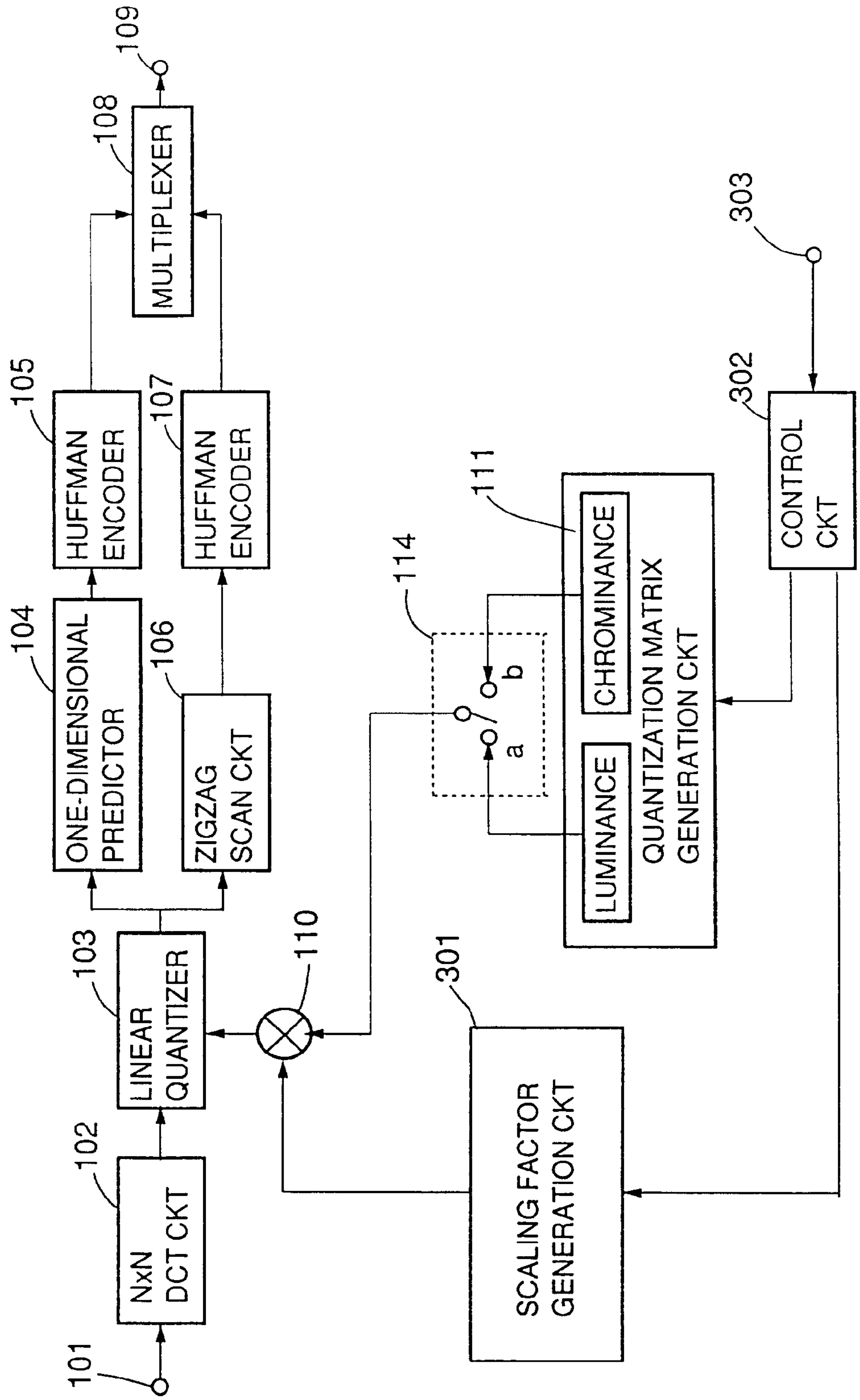

101
NxN DCT CKT
102
LINEAR QUANTIZER
103
ONE-DIMENSIONAL PREDICTOR
104
HUFFMAN ENCODER
105
ZIGZAG SCAN CKT
106
HUFFMAN ENCODER
107
MULTIPLEXER
108
109
110
114
a
b
LUMINANCE
CHROMINANCE
QUANTIZATION MATRIX GENERATION CKT
111
SCALING FACTOR GENERATION CKT
301
CONTROL CKT
302
303

FIG.4

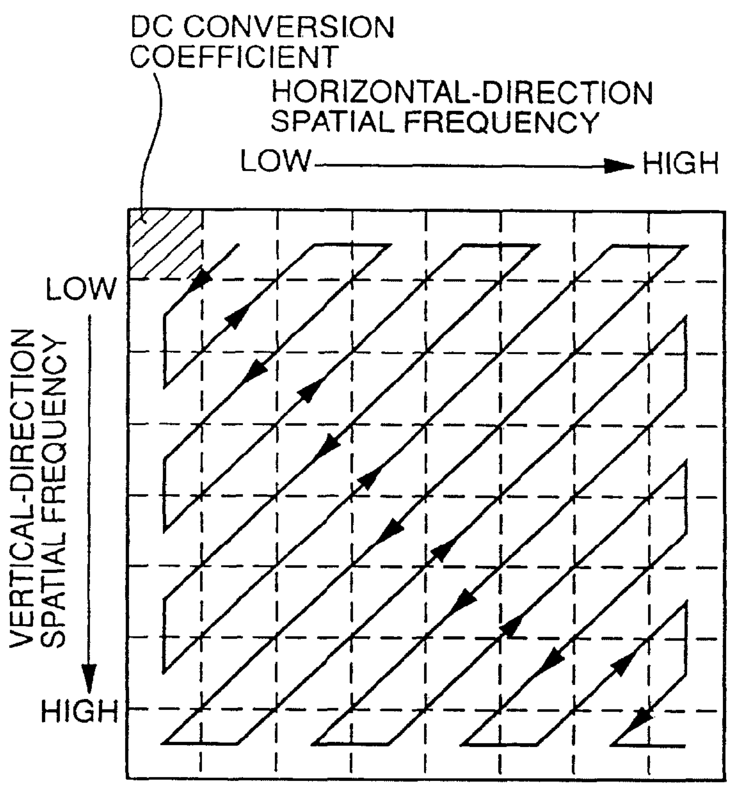

DC CONVERSION
COEFFICIENT
HORIZONTAL-DIRECTION
SPATIAL FREQUENCY
LOW
HIGH
VERTICAL-DIRECTION
SPATIAL FREQUENCY
LOW
HIGH

FIG.5

16	11	10	16	24	40	51	61
12	12	14	19	26	58	60	55
14	13	16	24	40	57	69	56
14	17	22	29	51	87	80	62
18	22	37	56	68	109	103	77
24	35	55	64	81	104	113	92
49	64	78	87	103	121	120	101
72	92	95	98	112	100	103	99

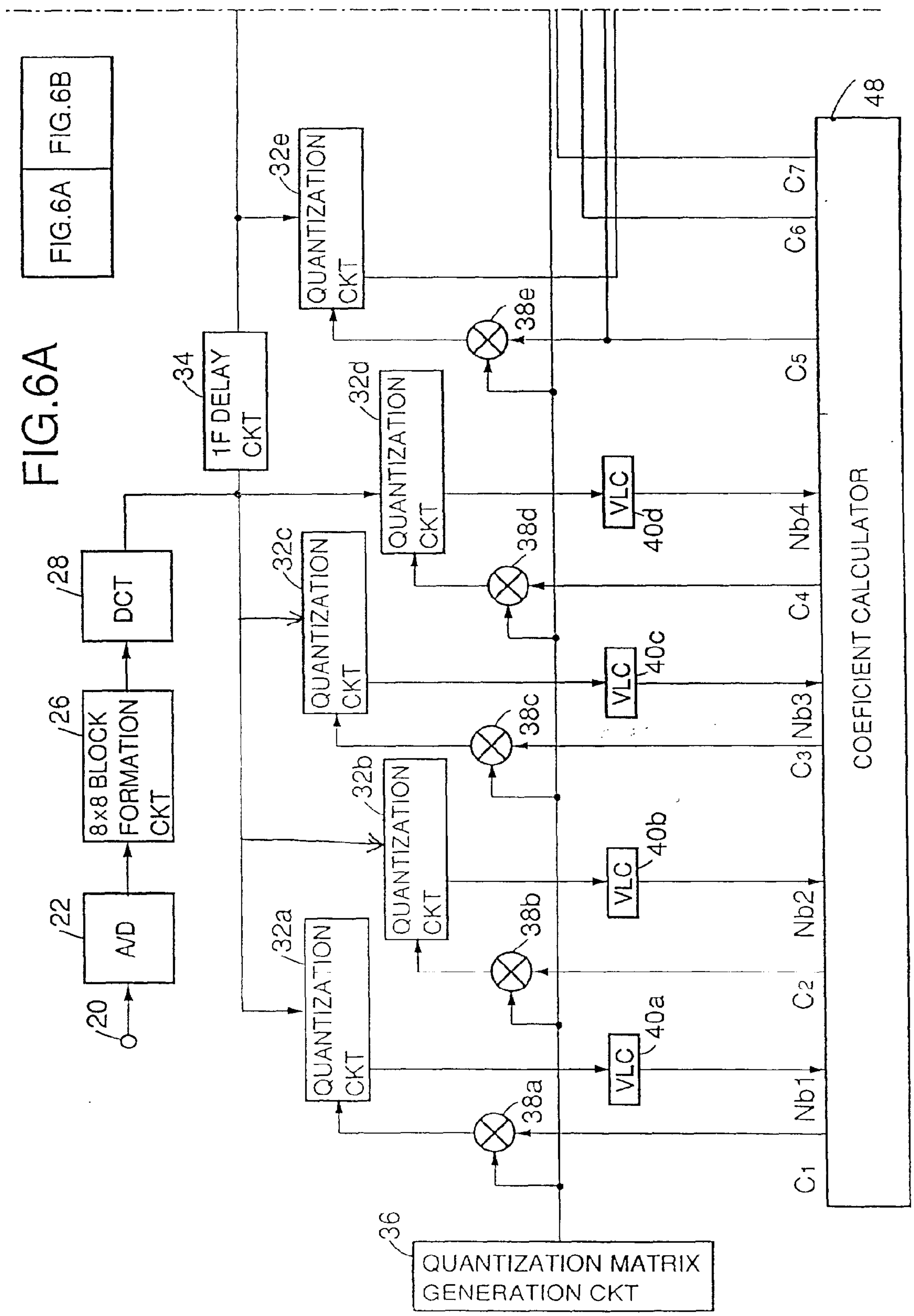
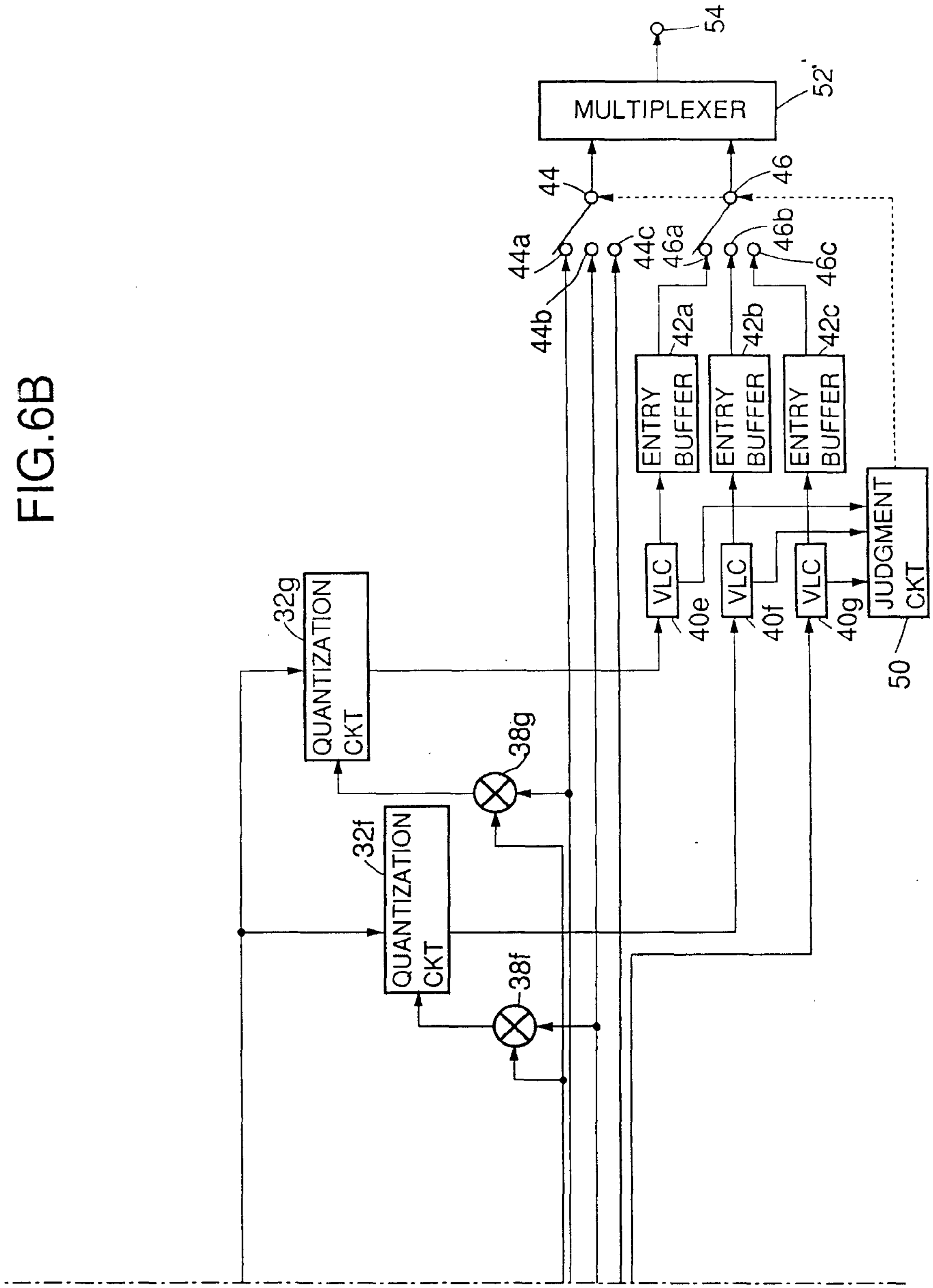


FIG.6A
FIG.6B
20
22
A/D
26
8x8 BLOCK FORMATION CKT
28
DCT
34
1F DELAY CKT
32a
32b
32c
32d
32e
QUANTIZATION CKT
QUANTIZATION CKT
QUANTIZATION CKT
QUANTIZATION CKT
QUANTIZATION CKT
38a
38b
38c
38d
38e
VLC
40a
VLC
40b
VLC
40c
VLC
40d
36
QUANTIZATION MATRIX GENERATION CKT
C1
Nb1
C2
Nb2
C3
Nb3
C4
Nb4
C5
C6
C7
COEFICIENT CALCULATOR
48

FIG.6A

FIG.6B


54
MULTIPLEXER
52'
44
46
44a
44b
44c
46a
46b
46c
ENTRY BUFFER
42a
ENTRY BUFFER
42b
ENTRY BUFFER
42c
VLC
40e
VLC
40f
VLC
40g
JUDGMENT CKT
50
QUANTIZATION CKT
32g
QUANTIZATION CKT
32f
38g
38f

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 746 159 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
31.07.2002 Bulletin 2002/31

(51) Int Cl.⁷: **H04N 7/26**, H04J 3/16, H04J 3/24, H04Q 11/04, G11B 20/12, H04N 7/62

(21) Application number: **96108798.8**

(22) Date of filing: **31.05.1996**

(54) **Moving-picture signal encoding and related decoding**

Bildbewegungssignalkodierung und entsprechende Dekodierung

Codage de signal d'image animée et décodage afférent

(84) Designated Contracting States:
BE DE ES FR GB IT

(30) Priority: **02.06.1995 JP 13705595**

(43) Date of publication of application:
04.12.1996 Bulletin 1996/49

(73) Proprietor: **MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.**
Kadoma-shi, Osaka-fu (JP)

(72) Inventors:
- **Machida, Yutaka**
Hodogaya-ku, Yokohama (JP)
- **Imura, Koji**
Hodogaya-ku, Yokohama (JP)

(74) Representative: **Tiedtke, Harro, Dipl.-Ing.**
Patentanwaltsbüro
Tiedtke-Bühling-Kinne & Partner
Bavariaring 4
80336 München (DE)

(56) References cited:
EP-A- 0 600 495
DE-A- 3 602 825
NL-A- 8 900 112
US-A- 4 876 698

EP 0 746 159 B1

Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention relates to a method and apparatus for encoding a moving-picture signal. This invention also relates to a method and apparatus for decoding an encoding-resultant signal back to an original moving-picture signal.

Description of the Prior Art

[0002] It is well-known that motion-compensated inter-frame predictive encoding enables the compression of a moving-picture signal. The motion-compensated inter-frame predictive encoding uses a temporal correlation in a moving picture. It is also well-known to use discrete cosine transform (DCT) in compressing a moving-picture signal. The DCT-based technique uses a spatial correlation in a moving picture.

[0003] According to a typical type of highly-efficient encoding of a moving-picture signal, a signal which results from DCT is quantized, and a quantization-resultant signal is subjected to an entropy encoding process. The entropy encoding process uses a statistical correlation in a moving picture, and enables the compression of the moving-picture signal.

[0004] In the typical type of highly-efficient encoding, every frame represented by a moving-picture signal is divided into blocks of a same size, and signal processing is executed block by block. A known way of increasing the ability to withstand signal errors, which occur during the transmission of moving-picture information, includes a step of providing groups each having a plurality of successive signal blocks, and a step of adding a sync signal to the head of every group. Such a block group corresponds to a slice defined in the MPEG 2 standards (the Moving Picture Experts Group 2 standards). The block group is also referred to as a GOB (a group of blocks).

[0005] Errors tend to occur in an information signal during the transmission thereof. A well-known way of enabling a reception side to correct such errors is that a transmission side adds an error correction signal to an information signal before the transmission of a resultant composite signal. The reception side extracts the error correction signal from the received composite signal, and corrects errors in the information signal in response to the extracted error correction signal.

[0006] Furthermore, from reference NL-A-8 900 112 it is known to insert into a data flow synchronization words at regular intervals. Furthermore, the data flow is grouped wherein a group contains one or more information words. In addition, encoding is performed by using a variable length encoding. Moreover, the synchronization words comprise a pointer indicating where the next information word group starts.

[0007] Reference DE-A-3 602 825 shows a method and a system for synchronization of TV signals when using digital broadcasting and data words with variable length. On side of the transmitter a sync data word and an distance data word are inserted at constant intervals wherein the distance data word indicates the distance in bit until the next line begins.

[0008] Reference US-A-4 876 698 discloses a system for transmitting sequences of digital samples encoded by variable-length binary words. There is shown a transmitter device comprising a statistic encoding circuit for encoding words of a fixed length, a synchronizing circuit for forming synchronizing words which define positions of the variable-length words and a multiplexer circuit for combining the synchronizing words with the variable-length words.

[0009] Furthermore, there is shown a receiver device which discloses a. demultiplexer circuit for applying from one of its outputs the variable-length words to a statistic decoding circuit and from its other the synchronizing words to a processing circuit the position of the samples.

[0010] Reference Ep-A-0 600 495 shows an apparatus for recording and reproducing a digital video signal wherein said video signal for one frame is converted into macro blocks which are arranged in a predetermined order to a rectangular block. The macro blocks are converted to synchronizing block data and are recorded in a predetermined number of tracks of a magnetic tape.

SUMMARY OF THE INVENTION

[0011] It is an object of the present invention to provide an improved method (apparatus) for encoding a moving-picture signal and for decoding an encoding-resultant signal back to an original moving picture signal, respectively.

[0012] This object is achieved by a method (apparatus) as outlined in the attached claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Fig. 1 is a diagram of an example of the structure of a bit sequence in a first embodiment of this invention.

[0014] Fig. 2 is a diagram of an example of the relation among a picture frame, transmission frames, and macro-blocks in the first embodiment of this invention.

[0015] Fig. 3 is a block diagram of an encoding apparatus in the first embodiment of this invention.

[0016] Fig. 4 is a block diagram of a framing processor in Fig. 3.

[0017] Fig. 5 is a block diagram of a decoding apparatus according to a second embodiment of this invention.

[0018] Fig. 6 is a block diagram of a sync signal detector in Fig. 5.

[0019] Fig. 7 is a block diagram of a signal generator in Fig. 5.

[0020] Fig. 8 is a block diagram of an encoding apparatus according to a third embodiment of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Embodiment

[0021] The QCIF (quarter common intermediate format) is used as a video format. According to the QCIF, every picture frame has 176 pixels by 144 pixels. In addition, every picture frame related to a luminance signal is divided into macro-blocks each having 16 pixels by 16 pixels. Further, every picture frame related to color difference signals is divided into macro-blocks each having 8 pixels by 8 pixels. An error correction signal uses a Bose and Ray-Chaudhuri (BCH) code of the (511, 493) type.

[0022] With reference to Fig. 1, a bit sequence representing a moving picture is divided into segments each having 476 successive bits. A 9-bit start address SA and an 8-bit location address LA are added to every bit-sequence segment. An 18-bit error correction signal EC is added to every 493-bit combination of a bit-sequence segment, a start address SA, and a location address LA. Every 511-bit combination of a bit-sequence segment, a start address SA, a location address LA, and an error correction signal EC constitutes one transmission frame (referred to as one group). In every transmission frame, a start address SA, a location address LA, a bit-sequence segment, and an error correction signal EC are sequentially arranged in the order. A 16-bit sync signal is added to every transmission frame. In a resultant bit sequence, sync signals are placed between transmission frames. The resultant bit sequence is transmitted from an encoding side to a decoding side.

[0023] The following conditions are now assumed. As shown in Fig. 1, a first transmission frame contains 1-st to 8-th macro-blocks and also a former part of a 9-th macro-block in a first block line. A second transmission frame contains a latter part of the 9-th macro-block and also 10-th and 11-th macro-blocks in the first block line.

[0024] The second transmission frame further contains 1-st to 11-th macro-blocks in a second block line, and a 1-st macro-block and also a former part of a 2-nd macro-block in a third block line. A third transmission frame contains a latter part of the 2-nd macro-block and also 3-rd to 9-th macro-blocks in the third block line. The third transmission frame further contains a former part of a 10-th macro-block in the third block line. Under these assumed conditions, the first, second, and third transmission frames occupy regions in a picture frame as shown in Fig. 2.

[0025] Terms, "a divided macro-block" and "an undivided macro-block", are now introduced. A divided macro-block means a macro-block divided into two parts which are in two successive transmission frames respectively. Under the conditions in Fig. 1, the 9-th macro-block in the first block line is an example of the divided macro-block. An undivided macro-block means a macro-block fully contained in one transmission frame. Under the conditions in Fig. 1, the 10-th macro-block in the first block line is an example of the undivided macro-block.

[0026] It is now further assumed that the latter part of the 9-th macro-block in the first block line which is contained in the second transmission frame has 40 bits. As shown in Fig. 1, the 40 bits in the latter part of the 9-th macro-block in the first block line follow the start address SA and the location address LA of the second transmission frame. In the second transmission frame, the 10-th macro-block in the first block line starts from a 58-th bit place with respect to the head of the second transmission frame since it is preceded by 57 bits composed of the 9-bit start address SA, the 8-bit location address LA, and the 40 bits of the 9-th macro-block. Accordingly, the start address SA of the second transmission frame is set to a state representing a bit place of "58" (the 58-th bit place) measured from the head of the second transmission frame. In addition, the location address LA of the second transmission frame is set to a state of [1, 10] which represents the "10-th" macro-block in the "1-st" block line.

[0027] It is now further assumed that the latter part of the 2-nd macro-block in the third block line which is contained in the third transmission frame has 80 bits. As shown in Fig. 1, the 80 bits in the latter part of the 2-nd macro-block in the third block line follow the start address SA and the location address LA of the third transmission frame. In the third transmission frame, the 3-rd macro-block in the third block line starts from a 98-th bit place with respect to the head of the third transmission frame since it is preceded by 97 bits composed of the 9-bit start address SA, the 8-bit location address LA, and the 80 bits of the 2-nd macro-block. Accordingly, the start address SA of the third transmission frame is set to a state representing a bit place of "98" (the 98-th bit place) measured from the head of the third transmission frame. In addition, the location address LA of the third transmission frame is set to a state of [3, 3] which represents the "3-rd" macro-block in the "3-rd" block line.

[0028] In this way, the start address SA of every transmission frame represents a bit position from which a first undivided macro-block starts. In addition, the location address LA of the transmission frame represents the position of the first undivided macro-block relative to the related picture frame.

[0029] As understood from the previous description, transmission frames corresponding to macro-block groups have a fixed length or a given number of bits. Accordingly, frames for the error correction process can be accorded with the macro-block group length. Thus, sync signals can be used in common for error-correction frames and macro-block group frames (transmission frames). This is advantageous in reducing an amount of used sync signals.

[0030] With reference to Fig. 3, an encoding apparatus includes a motion vector estimator 701 and an encoding-type deciding device 702 which receive an input signal 716 representing a moving picture. The encoding apparatus of Fig. 3 also includes a switch 703, a frame memory 704, an address controller 705, a subtracter 706, a discrete cosine transform (DCT) device 707, a quantizer 708, an inverse quantizer 709, an inverse DCT device 710, an adder 711, and an encoder 712.

[0031] The motion vector estimator 701 is connected to the frame memory 704, the address controller 705, and the encoder 712. The encoding-type deciding device 702 is connected to the switch 703, the frame memory 704, and the encoder 712. The switch 703 is connected to the frame memory 704, the subtracter 706, and the adder 711. The frame memory 704 is connected to the address controller 705 and the adder 711. The subtracter 706 receives the input picture signal 716. The subtracter 706 is connected to the DCT device 707. The DCT device 707 is connected to the quantizer 708. The quantizer 708 is connected to the inverse quantizer 709 and the encoder 712. The inverse quantizer 709 is connected to the inverse DCT device 710. The inverse DCT device 710 is connected to the adder 711.

[0032] The encoding apparatus of Fig. 3 further includes a framing processor 101, a multiplexer 714, and an error-correction-code adder 715. The framing processor 101 is connected to the encoder 712. The multiplexer 714 is connected to the framing processor 101. The error-correction-code adder 715 is connected to the multiplexer 714.

[0033] The motion vector estimator 701 receives the input picture signal 716 representing a current picture frame. The motion vector estimator 701 receives an output signal 718 of the frame memory 704 which represents an immediately preceding picture frame related to the input picture signal 716. The motion vector estimator 701 compares the current picture frame signal 716 and the immediately-preceding picture frame signal 718, thereby detecting a motion estimate (motion vectors) and outputting a signal 720 representing the detected motion estimate (the detected motion vectors). In other words, the motion vector estimator 701 functions to estimate a picture motion and generate a signal representing the estimated picture motion.

[0034] The address controller 705 receives the motion vector signal 720 from the motion vector estimator 701. The address controller 705 controls the frame memory 704 in response to the motion vector signal 720 so that the frame memory 704 outputs a motion-compensated predictive picture signal 719 corresponding to the input picture signal 716.

[0035] The encoding-type deciding device 702 receives the input picture signal 716. The encoding-type deciding device 702 receives the predictive picture signal 719 from the frame memory 704. The encoding-type deciding device 702 compares the input picture signal 716 and the predictive picture signal 719, thereby deciding which of an intra-frame encoding process and an inter-frame encoding process should be executed. The encoding-type deciding device 702 outputs an encoding mode signal 717 depending on the result of the decision.

[0036] The switch 703 has a movable contact and fixed contacts "a" and "b". The movable contact selectively touches either the fixed contact "a" or the fixed contact "b". The movable contact of the switch 703 is connected to the subtracter 706 and the adder 711. The fixed contact "a" of the switch 703 has no connection. The fixed contact "b" of the switch 703 is connected to the frame memory 704. The switch 703 is controlled by the encoding mode signal 717 outputted from the encoding-type deciding device 702. In the case where the encoding mode signal 717 represents that the intra-frame encoding process should be executed, the movable contact of the switch 703 is in touch with the fixed contact "a" thereof. Accordingly, in this case, the predictive picture signal 719 outputted by the frame memory 704 is inhibited from traveling to the subtracter 706 and the adder 711. In the case where the encoding mode signal 717 represents that the inter-frame encoding process should be executed, the movable contact of the switch 703 is in touch with the fixed contact "b" thereof. Accordingly, in this case, the predictive picture signal 719 is allowed to travel from the frame memory 704 to the subtracter 706 and the adder 711.

[0037] In the case where the inter-frame encoding process is selected, the subtracter 706 calculates the difference between the input picture signal 716 and the predictive picture signal 719. The subtracter 706 outputs an error signal representing the calculated difference. In the case where the intra-frame encoding process is selected, the input picture signal 716 passes through the subtracter 706 without being processed thereby.

[0038] The DCT device 707 receives the output signal of the subtracter 706. The DCT device 707 subjects the output signal of the subtracter 706 to discrete cosine transform (DCT), thereby outputting a signal representing DCT coefficients. Specifically, the DCT device 707 divides the output signal of the subtracter 706 into blocks each corresponding to, for example, 8 pixels by 8 pixels. The DCT is executed block by block. The quantizer 708 receives the DCT coefficient signal from the DCT device 707, and quantizes the DCT coefficient signal in accordance with a suitable quantization step size. The quantizer 708 outputs the quantization-resultant signal.

[0039] The encoder 712 receives the quantization-resultant signal from the quantizer 708. The encoder 712 receives the motion vector signal 720 from the motion vector estimator 701. The encoder 712 receives the encoding mode signal 717 from the encoding-type deciding device 702. The encoder 712 includes a first encoding section operating on the quantization-resultant signal, a second encoding section operating on the motion vector signal 720, a third encoding section operating on the encoding mode signal 717, and a multiplexing sec-

tion. Specifically, the device 712 encodes the quantization-resultant signal into corresponding words of a variable length code, that is, a first encoding-resultant signal. The device 712 encodes the motion vector signal 720 into corresponding words of a variable length code, that is, a second encoding-resultant signal. The device 712 encodes the encoding mode signal 717 into corresponding words of a variable length code, that is, a third encoding-resultant signal. The encoder 712 multiplexes the first encoding-resultant signal, the second encoding-resultant signal, and the third encoding-resultant signal into a bit sequence 102. The encoder 712 outputs the bit sequence 102.

[0040] The encoder 712 has a section for dividing the quantization-resultant signal into macro-blocks (MB). Accordingly, the bit sequence 102 is similarly divided into macro-blocks (MB). The encoder 712 executes the processing or the encoding of the quantization-resultant signal macro-block by macro-block. The encoder 712 further has a section for generating a signal 103 representing the end of the processing of every macro-block (MB). The encoder 712 outputs the MB end signal 103.

[0041] The inverse quantizer 709 receives the quantization-resultant signal from the quantizer 708. The device 709 subjects the quantization-resultant signal to an inverse quantization process, thereby recovering a DCT coefficient signal corresponding to the output signal of the DCT device 707. The inverse DCT device 710 receives the recovered DCT coefficient signal from the inverse quantizer 709. The device 710 subjects the recovered DCT coefficient signal to inverse DCT, thereby converting the DCT coefficient signal back to an error signal corresponding to the output signal of the subtracter 706. The inverse DCT device 710 outputs the error signal to the adder 711. In the case where the inter-frame encoding process is selected, the adder 711 receives the predictive picture signal 719 from the frame memory 704 and combines the error signal and the predictive picture signal 719 into a picture signal corresponding to the input picture signal 716. In the case where the intra-frame encoding process is selected, the error signal passes through the adder 711 without being processed thereby. In this way, the adder 711 recovers a picture signal corresponding to the input picture signal 716. The adder 711 outputs the recovered picture signal to the frame memory 704. The recovered picture signal is written into the frame memory 704. The frame memory 704 is controlled by the address controller 705, thereby generating the immediately-preceding picture frame signal 718 and the predictive picture signal 719 on the basis of the recovered picture signal.

[0042] The framing processor 101 receives the bit sequence 102 and the MB end signal 103 from the encoder 712. The bit sequence 102 passes through the framing processor 101 substantially without being processed thereby. The framing processor 101 generates a start address signal 104, a sync signal 105, and a location address signal 105 in response to the bit sequence 102 and the MB end signal 103. The start address signal 104 corresponds to a start address SA in Fig. 1. The sync signal 105 corresponds to a sync signal in Fig. 1. The location address signal 105 corresponds to a location address LA in Fig. 1.

[0043] The multiplexer 714 receives the bit sequence 102, the start address signal 104, the sync signal 105, and the location address signal 106 from the framing processor 101. The device 714 multiplexes the bit sequence 102, the start address signal 104, the sync signal 105, and the location address signal 106 into a first composite information signal. During the signal processing by the multiplexer 714, the bit sequence 102 is divided into transmission frames referred to as macro-block groups. The device 714 executes the multiplexing group by group (transmission-frame by transmission-frame).

[0044] The error-correction-code adder 715 receives the first composite information signal from the multiplexer 714. The device 715 adds an error correction signal or words of an error correction code to the first composite information signal, thereby converting the first composite information signal into a second composite information signal. The added error correction signal corresponds to an error correction signal EC in Fig. 1. The error-correction code adder 715 outputs the second composite information signal to a transmission line. The second composite information signal has a form shown in Fig. 1.

[0045] As shown in Fig. 4, the framing processor 101 includes counters 201 and 202, a comparator 203, and signal generators 204, 205, and 206. The counter 201 receives the MB end signal 103. The counter 201 executes an up-counting process, and specifically counts every macro-block in response to the MB end signal. The counter 201 generates a signal 207 representing the number of counted macro-blocks. The counter 201 outputs the MB count number signal 207. The counter 201 is reset for every picture frame. The counter 202 receives the bit sequence 102. The counter 202 executes an up-counting process, and specifically counts every bit in the bit sequence 102. The counter 202 generates a signal 208 representing the number of counted bits. The counter 202 outputs the bit count number signal 208. The comparator 203 receives the bit count number signal 208 from the counter 202. The comparator 203 is informed of a reference signal representing a fixed value corresponding to a given number of bits, for example, 476 bits. The device 203 compares the bit count number signal 208 with the reference signal, thereby deciding whether or not the number of counted bits reaches the given number of bits (for example, 476 bits). When the number of counted bits reaches the given number of bits, the comparator 203 outputs a comparison result signal 209 in a logic state of "1". Otherwise, the comparator 203 outputs a comparison result signal 209 in a logic state of "0". Generally, the bit count number signal 208 is reset in response to every change

of the comparison result signal 209 from "0" to "1".

[0046] The signal generator 205 receives the MB count number signal 207 from the counter 201. The signal generator 205 receives the comparison result signal 209 from the comparator 203. The signal generator 205 produces the location address signal 106 in response to the MB count number signal 207 and the comparison result signal 209. Specifically, for every transmission frame, the signal generator 205 calculates the horizontal and vertical positions of a first undivided macro-block relative to a related picture frame by referring to the MB count number signal 207 provided that the comparison result signal 209 is "1". Accordingly, for every transmission frame, the signal 106 produced by the device 205 represents an 8-bit location address LA corresponding to the horizontal and vertical positions of a first undivided macro-block relative to a related picture frame. The signal generator 206 receives the comparison result signal 209 from the comparator 203. The signal generator 206 produces the sync signal 105 with 16 bits in response to every change of the comparison result signal 209 from "0" to "1". The signal generator 204 receives the MB end signal 103. The signal generator 204 receives the bit count number signal 208 from the counter 202. The signal generator 204 receives the comparison result signal 209 from the comparator 203. The signal generator 204 produces the start address signal 104 in response to the MB end signal 103, the bit count number signal 208, and the comparison result signal 209. Specifically, the signal generator 204 samples the bit count number signal 208 at a timing provided by every change of the MB end signal 103 to an active state which immediately follows a 0-to-1 change of the comparison result signal 209. For every transmission frame, the sampled bit count number signal 208 represents a bit place from which a first undivided macro-block starts. The signal generator 204 outputs the sampled bit count number signal 208 as the start address signal 104. Accordingly, for every transmission frame, the signal 104 produced by the device 204 represents a 9-bit start address SA corresponding to a bit place from which a first undivided macro-block starts.

Second Embodiment

[0047] A second embodiment of this invention relates to decoding an information signal (a bit sequence) generated by and transmitted from the encoding apparatus of Fig. 3. An input information signal to be decoded has fixed-length transmission frames and sync signals alternating with each other (see Fig. 1). Every transmission frame has a first given number of successive bits, for example, 511 bits. Every sync signal has a second given number of successive bits, for example, 16 bits. In the signal decoding based on the second embodiment of this invention, every bit in an input information signal is counted, and a detection is made as to a sync signal for every third given number of successive bits (for example, 527 bits equal to 16 bits plus 511 bits).

[0048] When a sync signal is normally and correctly detected, an error correction process is started. In the case where a sync signal is not successfully detected, that is, in the case where a detected sync signal disagrees with a correct sync signal, the detected sync signal is compared with the correct sync signal to calculate the number of bits in the detected sync signal which disagree in logic state from corresponding bits in the correct sync signal. The calculated number of such error bits in the detected sync signal is compared with a predetermined threshold number (a predetermined threshold value). In the case where the number of error bits in the detected sync signal is equal to or smaller than the threshold number, a synchronization process is implemented and established in response to the detected sync signal, and then an error correction process is started. In the case where the number of error bits in the detected sync signal exceeds the threshold number, the synchronization process is inhibited from being implemented and established in response to the detected sync signal. In this case, a next sync signal is waited.

[0049] Regarding every transmission frame (every macro-block group) in a bit sequence which results from the error correction process, bits prior to the bit place represented by a start address SA are remaining bits in a final macro-block (a divided macro-block) in the immediately-preceding transmission frame. Accordingly, a decoding process on the immediately-preceding transmission frame continues to be executed on the bits prior the bit place represented by the start address SA in the current transmission frame. On the other hand, a bit in the place represented by the start address SA is a head of a first undivided macro-block in a picture-frame region denoted by a location address LA. Accordingly, a re-synchronization process is executed so that a new decoding process starts at a timing which corresponds to the head of the first undivided macro-block. The second embodiment of this invention offers the following advantages. Since an input information signal to be decoded has fixed-length transmission frames (fixed-length macro-block groups), it is possible to forcedly implement and establish synchronization even when a detected sync signal has an error or errors. A start address SA and a location address LA enable the fixed-length structure of transmission frames. It is possible to implement re-synchronization at a timing which corresponds to a head of a first undivided macro-block in a picture-frame region denoted by a location address LA. Since frames for the error correction process agree in length with transmission frames (macro-block groups), an uncorrectable error or errors in a transmission frame are inhibited from interfering with the decoding of other transmission frames.

[0050] With reference to Fig. 5, a decoding apparatus includes a sync signal detector 301 and an error correction device 302 which receive an input bit sequence 727A representing a moving picture. The decoding ap-

paratus of Fig. 5 also includes a signal separator 303, a signal generator 304, a decoder 305, an address controller 306, an inverse quantizer 709A, an inverse DCT device 710A, an adder 711A, and a frame memory 726A.

[0051] The sync signal detector 301 is connected to the error correction device 302, the signal separator 303, and the signal generator 304. The error correction device 302 is connected to the signal separator 303. The signal separator 303 is connected to the signal generator 304, the decoder 305, and the address controller 306. The signal generator 304 is connected to the decoder 305. The decoder 305 is connected to the address controller 306 and the inverse quantizer 709A. The address controller 306 is connected to the frame memory 726A. The inverse quantizer 709A is connected to the inverse DCT device 710A. The inverse DCT device 710A is connected to the adder 711A. The adder 711A is connected to the frame memory 726A.

[0052] The sync signal detector 301 receives the input bit sequence 727A. The device 301 detects every sync signal in the input bit sequence 727A, and generates a signal 307 representative of a sync detection flag in response to the detected sync signal. The sync signal detector 301 outputs the sync detection flag signal 307.

[0053] The error correction device 302 receives the input bit sequence 727A. The error correction device 302 receives the sync detection flag signal 307 from the sync signal detector 301. The error correction device 302 implements and establishes transmission-frame synchronization with respect to the input bit sequence 727A in response to the sync detection flag signal 307. For every transmission frame, the error correction device 302 subjects the input bit sequence 727A to an error correction process responsive to an error correction signal contained therein. Accordingly, the error correction device 302 converts the input bit sequence 727A into a correction-resultant bit sequence 308. The error correction device 302 outputs the correction-resultant bit sequence 308. In general, the correction-resultant bit sequence 308 is void of the error correction signal. The transmission-frame synchronization in the error correction process by the error correction device 302 is controlled in response to the sync detection flag signal 307.

[0054] The signal separator 303 receives the correction-resultant bit sequence 308 from the error correction device 302. The signal separator 303 receives the sync detection flag signal 307 from the sync signal detector 301. The signal separator 303 implements and establishes transmission-frame synchronization with respect to the correction-resultant bit sequence 308 in response to the sync detection flag signal 307. For every transmission frame, the signal separator 303 removes a sync signal from the correction-resultant bit sequence 308 in response to the sync detection flag signal 307, and separates the correction-resultant bit sequence 308 into a signal 309 representing a start address SA, a signal 312 representing a location address LA, and a signal (a bit sequence) 311 representing picture information. The signal separator 303 outputs the start address signal 309, the location address signal 312, and the bit sequence 311. The transmission-frame synchronization in the signal separation process by the signal separator 303 is controlled in response to the sync detection flag signal 307.

[0055] The signal generator 304 receives the sync detection flag signal 307 from the sync signal detector 301. The signal generator 304 receives the start address signal 309 from the signal separator 303. The signal generator 304 produces a signal 310 representative of a macro-block start flag (an MB start flag) in response to the sync detection flag signal 307 and the start address signal 309. The MB start flag signal 310 represents a timing at which a first undivided macro-block starts in every transmission frame. The signal generator 304 outputs the MB start flag signal 310.

[0056] The decoder 305 receives the bit sequence 311 from the signal separator 303. The decoder 305 receives the MB start flag signal 310 from the signal generator 304. The decoder 305 includes a demultiplexing section, a first decoding section, and a second decoding section. Specifically, the decoder 305 demultiplexes the bit sequence 311 into a first variable-length-code signal representative of DCT coefficient information and a second variable-length-code signal representative of motion vectors. The device 305 decodes the first variable-length-code signal back into a quantization-resultant signal (a quantization-resultant DCT coefficient signal) 728A. The device 305 decodes the second variable-length-code signal back into a motion vector signal 720A. The decoder 305 outputs the quantization-resultant signal 728A and the motion vector signal 720A. The decoder 305 implements and establishes transmission-frame re-synchronization regarding the demultiplexing process and the decoding process in response to the MB start flag signal 310. The transmission-frame re-synchronization enables a new decoding process to start at a timing corresponding to the head of a first undivided macro-block in every transmission frame.

[0057] The inverse quantizer 709A receives the quantization-resultant signal 728A from the decoder 305. The device 709A subjects the quantization-resultant signal 728A to an inverse quantization process, thereby recovering a DCT coefficient signal. The inverse quantizer 709A outputs the recovered DCT coefficient signal. The inverse DCT device 710A receives the recovered DCT coefficient signal from the inverse quantizer 709A. The device 710A subjects the recovered DCT coefficient signal to inverse DCT, thereby converting the DCT coefficient signal back to an error signal. The inverse DCT device 710A outputs the error signal.

[0058] The address controller 306 receives the location address signal 312 from the signal separator 303. The address controller 306 receives the motion vector signal 720A from the decoder 305. The address controller 306 controls the frame memory 726A in response to

the location address signal 312 and the motion vector signal 720A so that the frame memory 726A outputs a motion-compensated predictive picture signal.

[0059] The adder 711A receives the error signal from the inverse DCT device 710A. The adder 711A receives the predictive picture signal from the frame memory 726A. The adder 711A combines the error signal and the predictive picture signal into an original picture signal 729A. In this way, the adder 711A recovers the original picture signal 729A. The adder 711A outputs the recovered picture signal 729A.

[0060] The recovered picture signal 729A is transmitted from the adder 711A to the frame memory 726A before being written thereinto. The frame memory 726A is controlled by the address controller 306, thereby generating the predictive picture signal on the basis of the recovered picture signal 729A.

[0061] As shown in Fig. 6, the sync signal detector 301 includes a counter 401, a comparator 402, a detecting section 403, a processor 404, and a deciding section 405. The counter 401 receives the input bit sequence 727A. The counter 401 executes an up-counting process, and specifically counts every bit in the input bit sequence 727A. The counter 401 generates a signal 406 representing the number of counted bits. The counter 401 outputs the bit count number signal 406 to the comparator 402. The comparator 402 is informed of a reference signal representing a fixed value corresponding to a given number of bits, for example, 527 bits. The device 402 compares the bit count number signal 406 with the reference signal, thereby deciding whether or not the number of counted bits reaches the given number of bits (for example, 527 bits). When the number of counted bits reaches the given number of bits, the comparator 402 outputs a transmission-frame flag signal 407 in a logic state of "1". Otherwise, the comparator 402 outputs a transmission-frame flag signal 407 in a logic state of "0". Generally, the bit count number signal 406 is reset in response to every change of the transmission-frame flag signal 407 from "0" to "1".

[0062] The detecting section 403 receives the input bit sequence 727A. The detecting section 403 includes a comparator. The detecting section 403 compares 16 successive bits in the input bit sequence 727A with a predetermined 16-bit reference sync signal. The detecting section 403 generates a signal 408 representative of a sync flag and a signal 409 representative of the number of error bits in response to the result of the comparison. The sync flag signal 408 assumes "1" when the 16 successive bits in the input bit sequence 727A completely agree with the predetermined 16-bit reference sync signal. Otherwise, the sync flag signal 408 is "0". The error-bit number signal 409 represents the number of bits among the 16 bits in the input bit sequence 727A which disagree with the corresponding bits in the predetermined 16-bit reference sync signal. The detecting section 403 outputs the sync flag signal 408 and the error-bit number signal 409.

[0063] The processor 404 receives the error-bit number signal 409 from the detecting section 403. The processor 404 includes a comparator. The processor 404 is informed of a reference signal representing a predetermined threshold number (a predetermined threshold value). The processor 404 compares the number of error bits, which is represented by the error-bit number signal 409, with the threshold number. The processor 404 generates a signal 410 representative of a forced sync acquisition flag in response to the result of the comparison. In the case where the number of error bits is equal to or smaller than the threshold number, the forced sync acquisition flag signal 410 is "1". Otherwise, the forced sync acquisition flag signal 410 is "0". The processor 404 outputs the forced sync acquisition flag signal 410.

[0064] The deciding section 405 receives the transmission-frame flag signal 407 from the comparator 402. The deciding section 405 receives the sync flag signal 408 from the detecting section 403. The deciding section 405 receives the forced sync acquisition flag signal 410 from the processor 404. The deciding section 405 generates the sync detection flag signal 307 in response to the transmission-frame flag signal 407, the sync flag signal 408, and the forced sync acquisition flag signal 410. The deciding section 405 includes a logic gate array or a ROM. In the case where the deciding section 405 includes a ROM, predetermined states of the sync detection flag signal 307 are stored in storage segments of the ROM respectively, and the transmission-frame flag signal 407, the sync flag signal 408, and the forced sync acquisition flag signal 410 compose an address signal operating on the ROM. When the transmission-frame flag signal 407, the sync flag signal 408, and the forced sync acquisition flag signal 410 are "1", "1", and "1" respectively, the sync detection flag signal 307 is inhibited from being outputted. When the transmission-frame flag signal 407, the sync flag signal 408, and the forced sync acquisition flag signal 410 are "1", "1", and "0" respectively, the sync detection flag signal 307 is "1". When the transmission-frame flag signal 407, the sync flag signal 408, and the forced sync acquisition flag signal 410 are "1", "0", and "1" respectively, the sync detection flag signal 307 is "1". When the transmission-frame flag signal 407, the sync flag signal 408, and the forced sync acquisition flag signal 410 are "1", "0", and "0" respectively, the sync detection flag signal 307 is "0". When the transmission-frame flag signal 407, the sync flag signal 408, and the forced sync acquisition flag signal 410 are "0", "1", and "1" respectively, the sync detection flag signal 307 is inhibited from being outputted. When the transmission-frame flag signal 407, the sync flag signal 408, and the forced sync acquisition flag signal 410 are "0", "1", and "0" respectively, the sync detection flag signal 307 is "1". When the transmission-frame flag signal 407, the sync flag signal 408, and the forced sync acquisition flag signal 410 are "0", "0", and "1" respectively, the sync detection flag signal 307 is "0".

When the transmission-frame flag signal 407, the sync flag signal 408, and the forced sync acquisition flag signal 410 are "0", "0", and "0" respectively, the sync detection flag signal 307 is "0".

[0065] The sync detection flag signal 307 being "1" enables the synchronization process to be implemented and established. The sync detection flag signal 307 being "0" inhibits the synchronization process from being implemented and established. In the case where the synchronization process is inhibited, a next sync signal is waited.

[0066] As shown in Fig. 7, the signal generator 304 includes a controller 501, a counter 502, and a comparator 503. The controller 501 receives the sync detection flag signal 307 from the sync signal detector 301. The controller 501 includes flip flops or bistable circuits. When the sync detection flag signal 307 changes from "0" to "1", the controller 501 outputs a reset signal 504 to the counter 502. At the same time, the controller 501 starts outputting an enable signal 505 to the counter 502. The counter 502 receives a bit sync signal synchronized with the bit sequence 311 outputted from the signal separator 303. The counter 502 is reset in response to the reset signal 504. The enable signal 505 allows the counter 502 to execute an up-counting process. Specifically, the device 502 counts every bit in the bit sequence 311. The counter 502 generates a signal 506 representing the number of counted bits. The counter 502 outputs the bit count number signal 506 to the comparator 503. The comparator 503 receives the start address signal 309 from the signal separator 303. The device 503 compares the bit count number signal 506 with the start address signal 309, thereby deciding whether or not the number of counted bits reaches a given number corresponding to the start address signal 309. When the number of counted bits reaches the given number corresponding to the start address signal 309, the comparator 503 outputs the MB start flag signal 310 in a logic state of "1". Otherwise, the comparator 503 outputs the MB start flag signal 310 in a logic state of "0". The counter 502 and the comparator 503 cooperate to detect remaining bits in a divided macro-block extending over two successive transmission frames. In other words, the counter 502 and the comparator 503 cooperate to detect the start of a first undivided macro-block in the present transmission frame. The MB start flag signal 310 represents a timing at which a first undivided macro-block starts in every transmission frame. The controller 501 receives the MB start flag signal 310 from the comparator 503. The controller 501 interrupts the outputting of the enable signal 505 in response to every change of the MB start flag signal 310 from "0" to "1". Accordingly, the operation of the counter 502 is suspended each time the MB start flag signal 310 changes from "0" to "1".

Third Embodiment

[0067] A third embodiment of this invention uses a hierarchical encoding process. An input picture signal to be encoded is separated into DCT coefficient information and overhead information. The overhead information includes information of an encoding mode (an encoding type) and information of motion vectors. A first priority and a second priority are assigned to the overhead information and the DCT coefficient information respectively.

[0068] The overhead information is encoded into a variable-length-code signal referred to as a first bit sequence. Sync signals and error correction code signals are added to the first bit sequence. Accordingly, the first bit sequence, the sync signals, and the error correction code signals are combined into a second bit sequence. The second bit sequence is outputted to a transmission line.

[0069] The DCT coefficient information is encoded into a variable-length-code signal referred to as a third bit sequence. Sync signals and error correction code signals are added to the third bit sequence. Accordingly, the third bit sequence, the sync signals, and the error correction code signals are combined into a fourth bit sequence. The fourth bit sequence is outputted to a transmission line.

[0070] The number of bits composing the error correction code signals added to the overhead information (the first-priority information) is greater than the number of bits composing the error correction code signals added to the DCT coefficient information (second-priority information). Therefore, the overhead information (the first-priority information) is higher than the DCT coefficient information (the second-priority information) in ability to withstand an error or errors which occur during the transmission thereof.

[0071] A calculation is made as to the number of bits of the second bit sequence which occur per unit time interval, that is, the rate of the occurrence of bits in the second bit sequence. It should be noted that the second bit sequence relates to the overhead information. Also, a calculation is made as to the number of bits of the fourth bit sequence which occur per unit time interval, that is, the rate of the occurrence of bits in the fourth bit sequence. It should be noted that the fourth bit sequence relates to the DCT coefficient information. Subsequently, the rate of the occurrence of bits in the second and fourth bit sequences is calculated by summing the calculated rates concerning the second and fourth bit sequences respectively.

[0072] The variable-length encoding stage related to the DCT coefficient information follows a quantization stage which serves to quantize picture information in accordance with a variable quantization step size. The quantization step size is increased and decreased as the calculated rate of the occurrence of bits in the second and fourth bit sequences rises and drops respectively. The increase and the decrease in the quantization step size cause a drop and a rise in the rate of the occurrence of bits in the fourth bit sequence (the DCT co-

efficient information). Accordingly, the actual rate of the occurrence of bits in the second and fourth bit sequences is controlled and maintained at essentially a constant rate.

[0073] With reference to Fig. 8, an encoding apparatus includes a motion vector estimator 701 and an encoding-type deciding device 702 which receive an input signal 716 representing a moving picture. The encoding apparatus of Fig. 8 also includes a switch 703, a frame memory 704, an address controller 705, a subtracter 706, a discrete cosine transform (DCT) device 707, a quantizer 708B, an inverse quantizer 709, an inverse DCT device 710, an adder 711, and an encoder 712B.

[0074] The motion vector estimator 701 is connected to the frame memory 704, the address controller 705, and the encoder 712B. The encoding-type deciding device 702 is connected to the switch 703, the frame memory 704, and the encoder 712B. The switch 703 is connected to the frame memory 704, the subtracter 706, and the adder 711. The frame memory 704 is connected to the address controller 705 and the adder 711. The subtracter 706 receives the input picture signal 716. The subtracter 706 is connected to the DCT device 707. The DCT device 707 is connected to the quantizer 708B. The quantizer 708B is connected to the inverse quantizer 709 and the encoder 712B. The inverse quantizer 709 is connected to the inverse DCT device 710. The inverse DCT device 710 is connected to the adder 711.

[0075] The encoding apparatus of Fig. 8 further includes a sync signal generator 713, multiplexers 601 and 602, error-correction-code adders 603 and 604, a calculator 605, and a controller 606. The sync signal generator 713 is connected to the multiplexers 601 and 602. The multiplexers 601 and 602 are connected to the encoder 712B. The error-correction-code adders 603 and 604 are connected to the multiplexers 601 and 602 respectively. The calculator 605 is connected to the error-correction-code adders 603 and 604. The controller 606 is connected to the calculator 605. The controller 606 is also connected to the quantizer 708B.

[0076] The motion vector estimator 701 receives the input picture signal 716 representing a current picture frame. The motion vector estimator 701 receives an output signal 718 of the frame memory 704 which represents an immediately preceding picture frame related to the input picture signal 716. The motion vector estimator 701 compares the current picture frame signal 716 and the immediately-preceding picture frame signal 718, thereby detecting a motion estimate (motion vectors) and outputting a signal 720 representing the detected motion estimate (the detected motion vectors). In other words, the motion vector estimator 701 functions to estimate a picture motion and generate a signal representing the estimated picture motion.

[0077] The address controller 705 receives the motion vector signal 720 from the motion vector estimator 701. The address controller 705 controls the frame memory 704 in response to the motion vector signal 720 so that the frame memory 704 outputs a motion-compensated predictive picture signal 719 corresponding to the input picture signal 716.

[0078] The encoding-type deciding device 702 receives the input picture signal 716. The encoding-type deciding device 702 receives the predictive picture signal 719 from the frame memory 704. The encoding-type deciding device 702 compares the input picture signal 716 and the predictive picture signal 719, thereby deciding which of an intra-frame encoding process and an inter-frame encoding process should be executed. The encoding-type deciding device 702 outputs an encoding mode signal 717 depending on the result of the decision.

[0079] The switch 703 has a movable contact and fixed contacts "a" and "b". The movable contact selectively touches either the fixed contact "a" or the fixed contact "b". The movable contact of the switch 703 is connected to the subtracter 706 and the adder 711. The fixed contact "a" of the switch 703 has no connection. The fixed contact "b" of the switch 703 is connected to the frame memory 704. The switch 703 is controlled by the encoding mode signal 717 outputted from the encoding-type deciding device 702. In the case where the encoding mode signal 717 represents that the intra-frame encoding process should be executed, the movable contact of the switch 703 is in touch with the fixed contact "a" thereof. Accordingly, in this case, the predictive picture signal 719 outputted by the frame memory 704 is inhibited from traveling to the subtracter 706 and the adder 711. In the case where the encoding mode signal 717 represents that the inter-frame encoding process should be executed, the movable contact of the switch 703 is in touch with the fixed contact "b" thereof. Accordingly, in this case, the predictive picture signal 719 is allowed to travel from the frame memory 704 to the subtracter 706 and the adder 711.

[0080] In the case where the inter-frame encoding process is selected, the subtracter 706 calculates the difference between the input picture signal 716 and the predictive picture signal 719. The subtracter 706 outputs an error signal representing the calculated difference. In the case where the intra-frame encoding process is selected, the input picture signal 716 passes through the subtracter 706 without being processed thereby.

[0081] The DCT device 707 receives the output signal of the subtracter 706. The DCT device 707 subjects the output signal of the subtracter 706 to discrete cosine transform (DCT), thereby outputting a signal representing DCT coefficients. The quantizer 708B receives the DCT coefficient signal from the DCT device 707, and quantizes the DCT coefficient signal in accordance with a quantization step size represented by an output signal 612 of the controller 606. The quantizer 708B outputs the quantization-resultant signal 607.

[0082] The encoder 712B receives the quantization-resultant signal 607 from the quantizer 708B. The encoder 712B receives the motion vector signal 720 from the motion vector estimator 701. The encoder 712B re-

ceives the encoding mode signal 717 from the encoding-type deciding device 702. The encoder 712B includes a first encoding section operating on the quantization-resultant signal 607, a second encoding section operating on the motion vector signal 720, a third encoding section operating on the encoding mode signal 717, and a multiplexing section. Specifically, the device 712B encodes the quantization-resultant signal 607 into corresponding words of a variable length code, that is, a first encoding-resultant signal 608. The first encoding-resultant signal 608 is referred to as a bit sequence 608 representing DCT coefficient information. The device 712B encodes the motion vector signal 720 into corresponding words of a variable length code, that is, a second encoding-resultant signal. The device 712B encodes the encoding mode signal 717 into corresponding words of a variable length code, that is, a third encoding-resultant signal. The encoder 712B multiplexes the second encoding-resultant signal and the third encoding-resultant signal into a bit sequence 609 representing overhead information. The encoder 712B outputs the DCT coefficient information bit sequence 608 and the overhead information bit sequence 609.

[0083] The inverse quantizer 709 receives the quantization-resultant signal 607 from the quantizer 708B. The device 709 subjects the quantization-resultant signal 607 to an inverse quantization process, thereby recovering a DCT coefficient signal corresponding to the output signal of the DCT device 707. The inverse DCT device 710 receives the recovered DCT coefficient signal from the inverse quantizer 709. The device 710 subjects the recovered DCT coefficient signal to inverse DCT, thereby converting the DCT coefficient signal back to an error signal corresponding to the output signal of the subtracter 706. The inverse DCT device 710 outputs the error signal to the adder 711. In the case where the inter-frame encoding process is selected, the adder 711 receives the predictive picture signal 719 from the frame memory 704 and combines the error signal and the predictive picture signal 719 into a picture signal corresponding to the input picture signal 716. In the case where the intra-frame encoding process is selected, the error signal passes through the adder 711 without being processed thereby. In this way, the adder 711 recovers a picture signal corresponding to the input picture signal 716. The adder 711 outputs the recovered picture signal to the frame memory 704. The recovered picture signal is written into the frame memory 704. The frame memory 704 is controlled by the address controller 705, thereby generating the immediately-preceding picture frame signal 718 and the predictive picture signal 719 on the basis of the recovered picture signal.

[0084] The sync signal generator 713 periodically produces and outputs a sync signal 610. The multiplexer 601 receives the DCT coefficient information bit sequence 608 from the encoder 712B. The multiplexer 601 receives the sync signal 610 from the sync signal generator 713. The device 601 multiplexes the DCT coefficient information bit sequence 608 and the sync signal 610 into a first composite information signal. The error-correction-code adder 603 receives the first composite information signal from the multiplexer 601. The device 603 adds an error correction signal or words of an error correction code to the first composite information signal, thereby converting the first composite information signal into a second composite information signal. The error-correction-code adder 603 outputs the second composite information signal to a transmission line.

[0085] The multiplexer 602 receives the overhead information bit sequence 609 from the encoder 712B. The multiplexer 602 receives the sync signal 610 from the sync signal generator 713. The device 602 multiplexes the overhead information bit sequence 609 and the sync signal 610 into a third composite information signal. The error-correction-code adder 604 receives the third composite information signal from the multiplexer 602. The device 604 adds an error correction signal or words of an error correction code to the third composite information signal, thereby converting the third composite information signal into a fourth composite information signal. The error-correction-code adder 604 outputs the fourth composite information signal to a transmission line.

[0086] The number of bits composing the error correction code signal added to the third composite information signal (the overhead information or the first-priority information) is greater than the number of bits composing the error correction code signal added to the first composite information signal (the DCT coefficient information or the second-priority information). Therefore, the overhead information (the first-priority information) is higher than the DCT coefficient information (the second-priority information) in ability to withstand an error or errors which occur during the transmission thereof.

[0087] The calculator 605 receives the second composite information signal from the error-correction-code adder 603. The calculator 605 receives the fourth composite information signal from the error-correction-code adder 604. The device 605 calculates the number of bits of the second composite information signal which occur per unit time interval, that is, the rate of the occurrence of bits in the second composite information signal. It should be noted that the second composite information signal relates to the DCT coefficient information. Also, the device 605 calculates the number of bits of the fourth composite information signal which occur per unit time interval, that is, the rate of the occurrence of bits in the fourth composite information signal. It should be noted that the fourth composite information signal relates to the overhead information. Subsequently, the device 605 calculates the rate of the occurrence of bits in the second and fourth composite information signals by summing the calculated rates concerning the second and fourth composite information signals respectively. The calculator 605 outputs a signal 611 representing the calculated rate of the occurrence of bits in the second and fourth composite information signals.

[0088] The controller 606 receives the bit rate signal 611 from the calculator 605. The controller 606 generates the quantization step size signal 612 in response to the bit rate signal 611. The controller 606 outputs the quantization step size signal 612 to the quantizer 708B. Accordingly, the quantization step size used by the quantizer 708B is increased and decreased as the calculated rate of the occurrence of bits in the second and fourth composite information signals rises and drops respectively. The increase and the decrease in the quantization step size cause a drop and a rise in the rate of the occurrence of bits in the second composite information signal (the DCT coefficient information). Accordingly, the actual rate of the occurrence of bits in the second and fourth composite information signals is controlled and maintained at essentially a constant rate.

[0089] It should be noted that the controller 606 may include a ROM. In this case, predetermined states of the quantization step size signal 612 are stored in storage segments of the ROM respectively, and the bit rate signal 611 is used as an address signal operating on the ROM.

Claims

1. A method of encoding a picture signal, comprising the steps of:

   dividing an input picture signal into blocks **(1-11);**
   grouping the blocks into groups **(BLOCK LINE)** each having a plurality of blocks;
   encoding the input picture signal into a second picture signal block by block, the second picture signal using a variable length code;
   dividing the second picture signal into transmission frames **(TRANSMIT FRAME)** each having a fixed number of bits;
   adding, to each of the transmission frames, a sync signal **(Sync)** and a signal of a start address **(SA),** the start address representing a position of a bit from which a specific block starts;

   characterized by the further step of:

   adding, to each of the transmission frames, an error correction signal **(EC)** and a signal of a location address **(LA)** representing a spatial position of the specific block within a related group thereby defining the position of the specific block relative to the related group of the input picture signal and the position of the related group within the input picture signal, the specific block being the first undivided block fully contained in the transmission frame.

2. A method according to claim 1, **characterized in that** each of the groups has a fixed number of bits.

3. A method of decoding a bit sequence comprising the steps of:

   detecting a sync signal **(Sync)** in an input bit sequence;
   detecting a signal of a start address **(SA)** in the input bit sequence in response to the detected sync signal;
   recognizing a bit in the input bit sequence as a start bit in response to the start address; and
   decoding the input bit sequence in response to a result of said recognizing;

   characterized in that
   said detecting step comprises the step of detecting a signal of a location address **(LA)** in the input bit sequence; and
   said recognizing step comprises the step of recognizing said start bit within a specific block in the input bit sequence as a start bit within the specific block in response to the location address and the start address, the bit being denoted by the start address, the specific block being denoted by the location address **(LA)** representing a spatial position of the specific block within a related group thereby defining the position of the specific block relative to the related group of the input picture signal and the position of the related group within the input picture signal, the specific block being the first undivided block fully contained in the transmission frame.

4. A method according to claim 3, **characterized in that** the sync-signal detecting step comprises detecting a sync signal in the input bit sequence for each fixed number of bits, calculating a number of errors in the detected sync signal, comparing the calculated number of errors with a predetermined reference number, and regarding the detected sync signal as a correct sync signal when the calculated number of errors is smaller than the predetermined reference number.

5. An apparatus for encoding a picture signal, comprising:

   means **(101)** for dividing an input picture signal into blocks;
   means **(714)** for grouping the blocks into groups each having a plurality of blocks;
   means **(712)** for encoding the input picture signal into a second picture signal block by block, the second picture signal using a variable length code;
   means **(203)** for dividing the second picture signal into transmission frames **(TRANSMIT FRAME)** each having a fixed number of bits;

and

means **(204, 206)** for adding, to each of the transmission frames, a sync signal **(Sync)** and a signal of a start address **(SA),** the start address representing a position of a bit from which a specific block starts;

characterized by

means **(205)** for adding, to each of the transmission frames, an error correction signal **(EC)** and a signal of a location address **(LA)** representing a spatial position of the specific block within a related group thereby defining the position of the specific block relative to the related group of the input picture signal and the position of the related group within the input picture signal, the specific block being the first undivided block fully contained in the transmission frame.

6. An apparatus for decoding a bit sequence comprising:

means **(301)** for detecting a sync signal in an input bit sequence;

means **(304)** for detecting a signal of a start address **(309)** in the input bit sequence in response to the detected sync signal;

means **(304)** for recognizing a bit in the input bit sequence as a start bit in response to the start address; and

means **(305)** for decoding the input bit sequence in response to a result of said recognizing means;

characterized by

means **(302)** for calculating a number of errors in the detected sync signal;

means **(302)** for comparing the calculated number of errors with a predetermined reference number;

means **(302)** for regarding the detected sync signal as a correct sync signal when the comparing means decides that the calculated number of errors is smaller than the predetermined reference number;

said detecting means further detecting a signal of a location address **(312)** in the input bit sequence in response to the detected sync signal which is regarded as the correct sync signal; and

said recognizing means recognizing said start bit within a specific block in the input bit sequence as a start bit within the specific block in response to the location address and the start address, the bit being denoted by the start address, the specific block being denoted by the location address **(LA)** representing a spatial position of the specific block within a related group thereby defining the position of the specific block relative to the related group of the input picture signal and the position of the related group within the input picture signal, the specific block being the first undivided block fully contained in the transmission frame.

Patentansprüche

1. Verfahren zum Codieren eines Bildsignals, mit den Verfahrensschritten:

Einteilen eines eingegebenen Bildsignals in Blöcke (1-11);

Gruppieren der Blöcke in Gruppen (BLOCK LINE), die jeweils über eine Vielzahl von Blöcken verfügen;

Codieren des eingegebenen Bildsignals blockweise in ein zweites Bildsignal, wobei das zweite Bildsignal einen längenvariablen Code verwendet;

Einteilen des zweiten Bildsignals in Übertragungsrahmen (TRANSMIT FRAME), die jeweils über eine feststehende Anzahl von Bits verfügen;

Addieren zu einem jeden der Übertragungsrahmen eines Synchronsignals (Sync) und eines Signals einer Startadresse (SA), die eine Position eines Bit aus einem spezifischen Block startet;

gekennzeichnet durch die weiteren Verfahrensschritte:

Addieren zu einem jeden der Übertragungsrahmen eines Fehlerkorrektursignals (EC) und eines Signals einer Ortsadresse (LA), die eine Raumposition im spezifischen Block innerhalb einer bezogenen Gruppe repräsentiert, **durch** eine Position des spezifischen Blockes, der bezüglich der bezogenen Gruppe des eingegebenen Bildsignals und der Position der bezogenen Gruppe innerhalb des eingegebenen Bildsignals festgelegt ist, wobei der spezifische Block der erste ungeteilte Block ist, der im Übertragungsrahmen vollständig enthalten ist.

2. Verfahren nach Anspruch 1, **dadurch gekennzeichnet, daß** jede der Gruppen eine feststehende Anzahl von Bits hat.

3. Verfahren zum Decodieren einer Bitsequenz, mit den Verfahrensschritten:

Feststellen eines Synchronsignals (Sync) in einer eingegebenen Bitsequenz;

Feststellen eines Signals einer Startadresse (SA) in der eingegebenen Bitsequenz als Reaktion auf das festgestellte Synchronsignal;

Erkennen eines Bits in der eingegebenen Bitsequenz als ein Startbit als Reaktion auf die Startadresse; und
Decodieren der eingegebenen Bitsequenz als Reaktion auf ein Ergebnis des Erkennens;

dadurch gekennzeichnet, daß
der Verfahrensschritt des Feststellens über den Schritt des Feststellens eines Signals einer Ortsadresse (LA) in der eingegebenen Bitsequenz verfügt; und
wobei der Verfahrensschritt des Erkennens über den Verfahrensschritt des Erkennens vom Startbit innerhalb eines spezifischen Blockes in der eingegebenen Bitsequenz als ein Startbit innerhalb des spezifischen Blockes als Reaktion auf die Ortsadresse und die Startadresse verfügt, wobei das Bit von der Startadresse bezeichnet ist, wobei die Ortsadresse (LA) den spezifischen Block bezeichnet, die eine Raumposition des spezifischen Blockes innerhalb einer jeweiligen Gruppe repräsentiert, wodurch die Position des spezifischen Blockes relativ zur jeweiligen Gruppe des eingegebenen Bildsignals und die Position der jeweiligen Gruppe innerhalb des eingegebenen Bildsignals festgelegt ist, wobei der spezifische Block der erste ungeteilte Block ist, der vollständig im Übertragungsrahmen enthalten ist.

4. Verfahren nach Anspruch 3, **dadurch gekennzeichnet, daß** der Verfahrensschritt des Feststellens vom Synchronsignal die weiteren Schritte umfaßt: Feststellen eines Synchronsignals in der eingegebenen Bitsequenz für jede feststehende Anzahl von Bits, Errechnen einer Anzahl von Fehlern im festgestellten Synchronsignal, Vergleichen der errechneten Anzahl von Fehlern mit einer vorbestimmten Bezugsanzahl und Betrachten des festgestellten Synchronsignals als ein korrektes Synchronsignal, wenn die errechnete Anzahl von Fehlern kleiner ist als die vorbestimmte Bezugsanzahl.

5. Vorrichtung zum Codieren eines Bildsignals, mit:

einem Mittel (101) zum Einteilen eines eingegebenen Bildsignals in Blöcke;
einem Mittel (714) zum Gruppieren der Blöcke in Gruppen, die jeweils über eine Vielzahl von Blöcken verfügen;
einem Mittel (712) zum Codieren des eingegebenen Bildsignals blockweise in ein zweites Bildsignal, das einen längenvariablen Code verwendet;
einem Mittel (203) zum Einteilen des zweiten Bildsignals in Übertragungsrahmen (TRANSMIT FRAME), die jeweils über eine feststehende Anzahl von Bits verfügen; und mit
einem Mittel (204, 206) zum Addieren zu einem jeden der Übertragungsrahmen eines Synchronsignals (Sync) und eines Signals einer Startadresse (SA), die eine Position eines Bits repräsentiert, von der ein spezifischer Block startet;

gekennzeichnet durch:

ein Mittel (205) zum Addieren zu einem jeden der Übertragungsbilder eines Fehlerkorrektursignals (EC) und eines Signals einer Ortsadresse (LA), die eine Raumposition vom spezifischen Block innerhalb einer jeweiligen Gruppe repräsentiert, wodurch die Position des spezifischen Blockes bezüglich der jeweiligen Gruppe vom eingegebenen Bildsignal festgelegt ist und die Position der jeweiligen Gruppe innerhalb des eingegebenen Bildsignals, wobei der spezifische Block der erste ungeteilte Block ist, der im Übertragungsrahmen vollständig enthalten ist.

6. Vorrichtung zum Decodieren einer Bitsequenz, mit:

einem Mittel (301) zum Feststellen eines Synchronsignals in einer eingegebenen Bitsequenz;
einem Mittel (304) zum Feststellen eines Signals einer Startadresse (309) in der eingegebenen Bitsequenz als Reaktion auf das festgestellte Synchronsignal;
einem Mittel (304) zum Erkennen eines Bits in der eingegebenen Bitsequenz als ein Startbit als Reaktion auf die Startadresse; und mit
einem Mittel (305) zum Decodieren der eingegebenen Bitsequenz als Reaktion auf ein Ergebnis des Erkennmittels;
gekennzeichnet durch
ein Mittel (302) zum Errechnen der Anzahl von Fehlern im festgestellten Synchronsignal;
einem Mittel (302) zum Vergleichen der errechneten Anzahl von Fehlern innerhalb einer vorbestimmten Bezugsanzahl;
einem Mittel (302) zum Ansehen des festgestellten Synchronsignals als korrektes Synchronsignal, wenn das Vergleichsmittel entscheidet, daß die errechnete Anzahl von Fehlern geringer als die vorbestimmte Bezugsanzahl ist;

wobei das Feststellmittel des weiteren ein Signal einer Ortsadresse (312) in der eingegebenen Bitsequenz als Reaktion auf das festgestellte Synchronsignal feststellt, das als korrektes Synchronsignal erkannt ist; und
wobei das Erkennmittel das Startbit innerhalb eines spezifischen Blockes in der eingegebenen Bitsequenz als ein Startbit innerhalb eines spezifi-

schen Blockes als Reaktion auf die Ortsadresse und die Startadresse erkennt, wobei die Startadresse das Bit benennt, wobei die Ortsadresse (LA) den spezifischen Block benennt, die eine Raumposition des spezifischen Blockes innerhalb einer jeweiligen Gruppe repräsentiert, wodurch die Position des spezifischen Blockes bezüglich der jeweiligen Gruppe vom eingegebenen Bildsignal und der Position der jeweiligen Gruppe innerhalb des eingegebenen Bildsignals festgelegt ist, wobei der spezifische Block der ungeteilte Block ist, der vollständig im Übertragungsrahmen enthalten ist.

Revendications

1. Procédé de codage d'un signal d'image, comprenant les étapes consistant à :

diviser un signal d'image d'entrée en blocs (1 à 11),
regrouper les blocs en groupes (LIGNE DE BLOCS) chacun comportant une pluralité de blocs,
coder le signal d'image d'entrée en un second signal d'image bloc par bloc, le second signal d'image utilisant un code à longueur variable,
diviser le second signal d'image en des trames d'émission (TRAME D'EMISSION) comportant chacune un nombre fixe de bits,
ajouter, à chacune des trames d'émission, un signal de synchronisation (Sync) et un signal d'une adresse de début (SA) l'adresse de début représentant une position d'un bit à partir duquel débute un bloc spécifique,

caractérisé par l'étape supplémentaire consistant à :

ajouter, à chacune des trames d'émission, un signal de correction d'erreur (EC) et un signal d'adresse d'emplacement (LA) représentant une position dans l'espace du bloc spécifique à l'intérieur d'un groupe associé en définissant ainsi la position du bloc spécifique par rapport au groupe associé du signal d'image d'entrée et la position du groupe associé à l'intérieur du signal d'image d'entrée, le bloc spécifique étant le premier bloc non divisé complètement contenu dans la trame d'émission.

2. Procédé selon la revendication 1, **caractérisé en ce que** chacun des groupes présente un nombre fixe de bits.

3. Procédé de décodage d'une séquence de bits comprenant les étapes consistant à :

détecter un signal de synchronisation (Sync) dans une séquence de bits d'entrée,
détecter un signal d'une adresse de début (SA) dans la séquence de bits d'entrée en réponse au signal de synchronisation détecté,
reconnaître un bit dans la séquence de bits d'entrée en tant que bits de début en réponse à l'adresse de début, et
décoder la séquence de bits d'entrée en réponse à un résultat de ladite reconnaissance,

caractérisé en ce que

ladite étape de détection comprend l'étape consistant à détecter un signal d'une adresse d'emplacement (LA) dans la séquence de bits d'entrée, et
ladite étape de reconnaissance comprend l'étape consistant à :

reconnaître ledit bit de début à l'intérieur d'un bloc spécifique dans la séquence de bits d'entrée en tant que bit de début à l'intérieur du bloc spécifié en réponse à l'adresse d'emplacement et à l'adresse de début, le bit étant repéré par l'adresse de début, le bloc spécifique étant repéré par l'adresse d'emplacement (LA) représentant une position dans l'espace du bloc spécifique à l'intérieur d'un groupe associé en définissant ainsi la position du bloc spécifique par rapport au groupe associé du signal d'image d'entrée et à la position du groupe associé à l'intérieur du signal d'image d'entrée, le bloc spécifique étant le premier bloc non divisé complètement contenu dans la trame d'émission.

4. Procédé selon la revendication 3, **caractérisé en ce que** l'étape de détection de signal de synchronisation comprend la détection d'un signal de synchronisation dans la séquence de bits d'entrée pour chaque nombre fixe de bits, le calcul d'un nombre d'erreurs dans le signal de synchronisation détecté, la comparaison du nombre calculé des erreurs à un nombre de référence prédéterminé, et la prise en considération du signal de synchronisation détecté en tant que signal de synchronisation correct lorsque le nombre des erreurs calculé est plus petit que le nombre de référence prédéterminé.

5. Dispositif destiné à coder un signal d'image, comprenant :

un moyen (101) destiné à diviser un signal d'image d'entrée en blocs,
un moyen (714) destiné à regrouper les blocs en groupes, chacun comportant une pluralité de blocs,
un moyen (712) destiné à coder le signal d'image d'entrée en un second signal d'image bloc

par bloc, le second signal d'image utilisant un code à longueur variable,

un moyen (203) destiné à diviser le second signal d'image en des trames d'émission (TRAME D'EMISSION) comportant chacune un nombre fixe de bits, et

un moyen (204, 206) destiné à additionner, pour chacune des trames d'émission, un signal de synchronisation (Sync) et un signal d'une adresse de début (SA) l'adresse de début représentant une position d'un bit à partir duquel débute un bloc spécifique,

caractérisé par

un moyen (205) destiné à ajouter, à chacune des trames d'émission, un signal de correction d'erreur (EC) et un signal d'une adresse d'emplacement (LA) représentant une position dans l'espace du bloc spécifique à l'intérieur d'un groupe associé en définissant ainsi la position du bloc spécifique par rapport au groupe associé du signal d'image d'entrée et à la position du groupe associé à l'intérieur du signal d'image d'entrée, le bloc spécifique étant le premier bloc non divisé complètement contenu dans la trame d'émission.

6. Dispositif destiné à décoder une séquence de bits comprenant :

un moyen (301) destiné à détecter un signal de synchronisation dans une séquence de bits d'entrée,

un moyen (304) destiné à détecter un signal d'une adresse de début (309) dans la séquence de bits d'entrée en réponse au signal de synchronisation détecté,

un moyen (304) destiné à reconnaître un bit dans la séquence de bits d'entrée en tant que bit de début en réponse à l'adresse de début, et

un moyen (305) destiné à décoder la séquence de bits d'entrée en réponse à un résultat dudit moyen de reconnaissance,

caractérisé par

un moyen (302) destiné à calculer un nombre d'erreurs dans le signal de synchronisation détecté,

un moyen (302) destiné à comparer le nombre calculé d'erreur avec un nombre de référence prédéterminé,

un moyen (302) destiné à considérer le signal de synchronisation détecté comme un signal de synchronisation correct lorsque le moyen de comparaison définit que le nombre d'erreurs calculé est plus petit que le nombre de référence prédéterminé,

ledit moyen de détection détectant en outre un signal d'une adresse d'emplacement (312) dans la séquence de bits d'entrée en réponse au signal de synchronisation détecté qui est considéré comme étant le signal de synchronisation correct, et

ledit moyen de reconnaissance reconnaissant ledit bit de début à l'intérieur d'un bloc spécifique de la séquence de bits d'entrée en tant que bit de début à l'intérieur du bloc spécifique en réponse à l'adresse d'emplacement et à l'adresse de début, le bit étant repéré par l'adresse de début, le bloc spécifique étant repéré par l'adresse d'emplacement (LA) représentant une position dans l'espace du bloc spécifique à l'intérieur d'un groupe associé en définissant ainsi la position du bloc spécifique par rapport au groupe associé du signal d'image d'entrée et la position du groupe associé à l'intérieur du signal d'image d'entrée, le bloc spécifique étant le premier bloc non divisé complètement contenu dans la trame d'émission.

FIG. 1

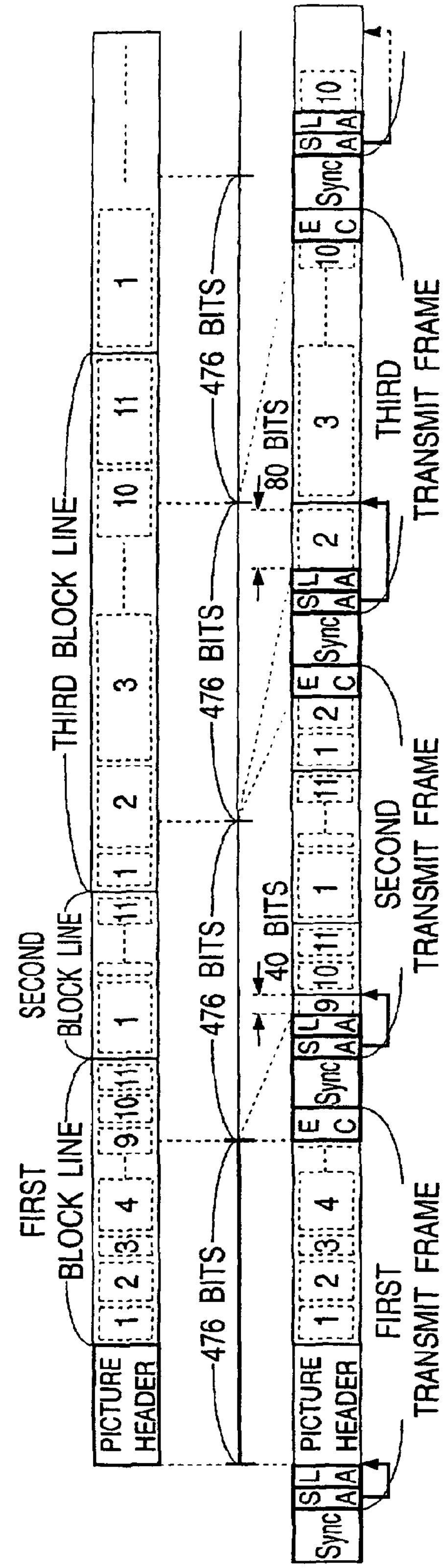
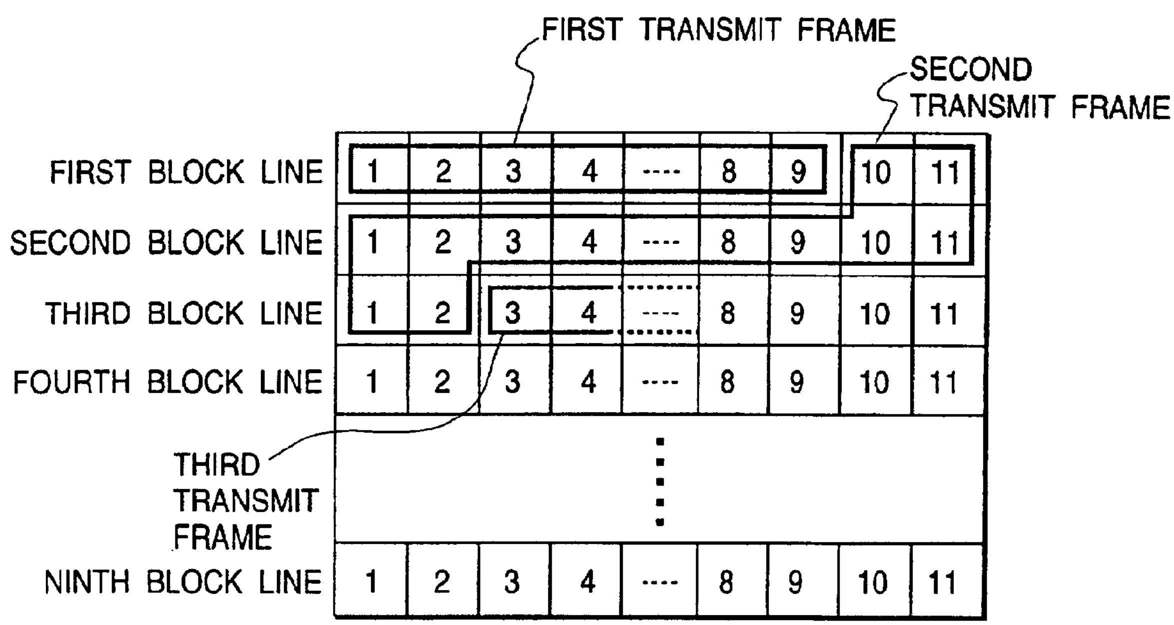
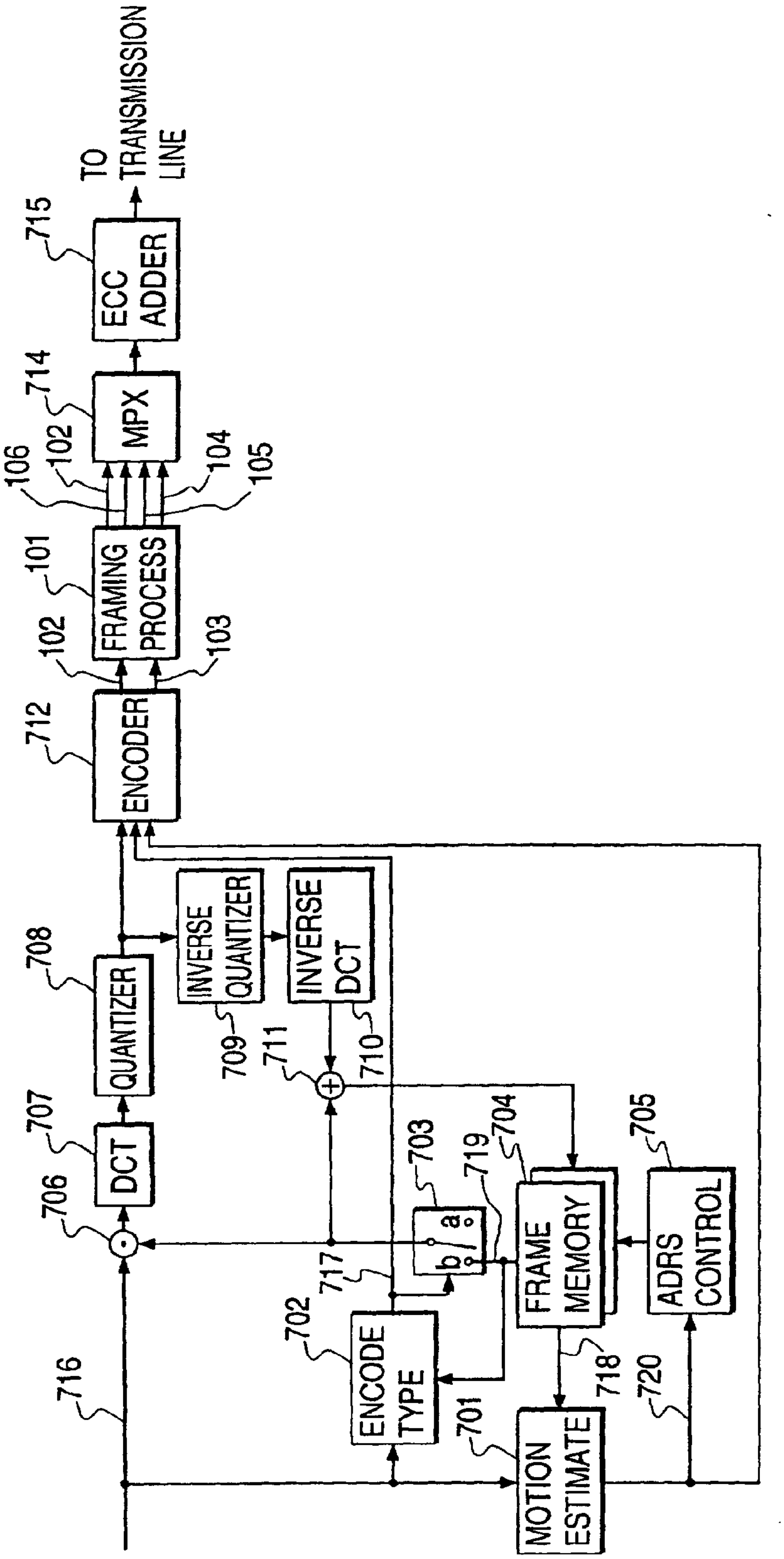

FIRST BLOCK LINE
SECOND BLOCK LINE
THIRD BLOCK LINE
PICTURE HEADER
476 BITS
40 BITS
80 BITS
Sync
SA
LA
EC
FIRST TRANSMIT FRAME
SECOND TRANSMIT FRAME
THIRD TRANSMIT FRAME

FIG. 2


FIRST TRANSMIT FRAME
SECOND TRANSMIT FRAME
FIRST BLOCK LINE
SECOND BLOCK LINE
THIRD BLOCK LINE
FOURTH BLOCK LINE
THIRD TRANSMIT FRAME
NINTH BLOCK LINE
1
2
3
4

8
9
10
11

FIG. 3



TO TRANSMISSION LINE
ECC ADDER
MPX
FRAMING PROCESS
ENCODER
QUANTIZER
DCT
INVERSE QUANTIZER
INVERSE DCT
FRAME MEMORY
ADRS CONTROL
ENCODE TYPE
MOTION ESTIMATE
b
a
715
714
106
102
104
105
101
103
712
708
707
706
709
711
710
703
719
704
705
702
717
716
701
718
720

FIG. 4

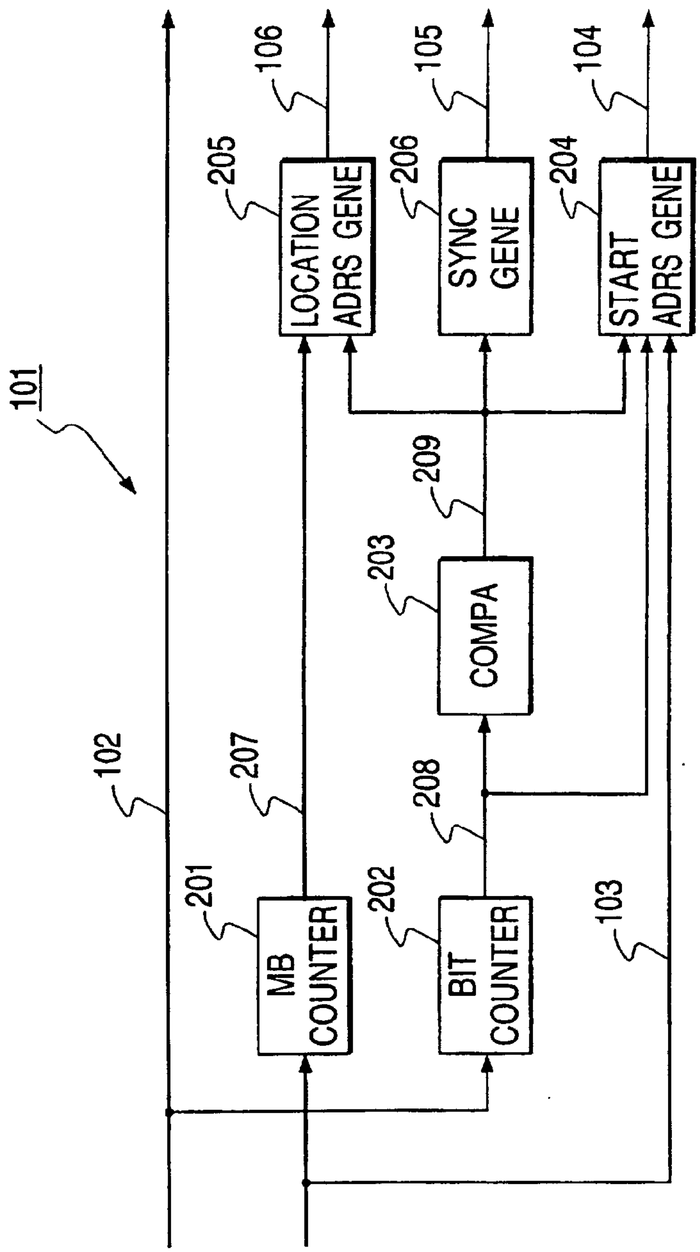

101
102
207
208
209
103
201
MB COUNTER
202
BIT COUNTER
203
COMPA
205
LOCATION ADRS GENE
206
SYNC GENE
204
START ADRS GENE
106
105
104

FIG. 5

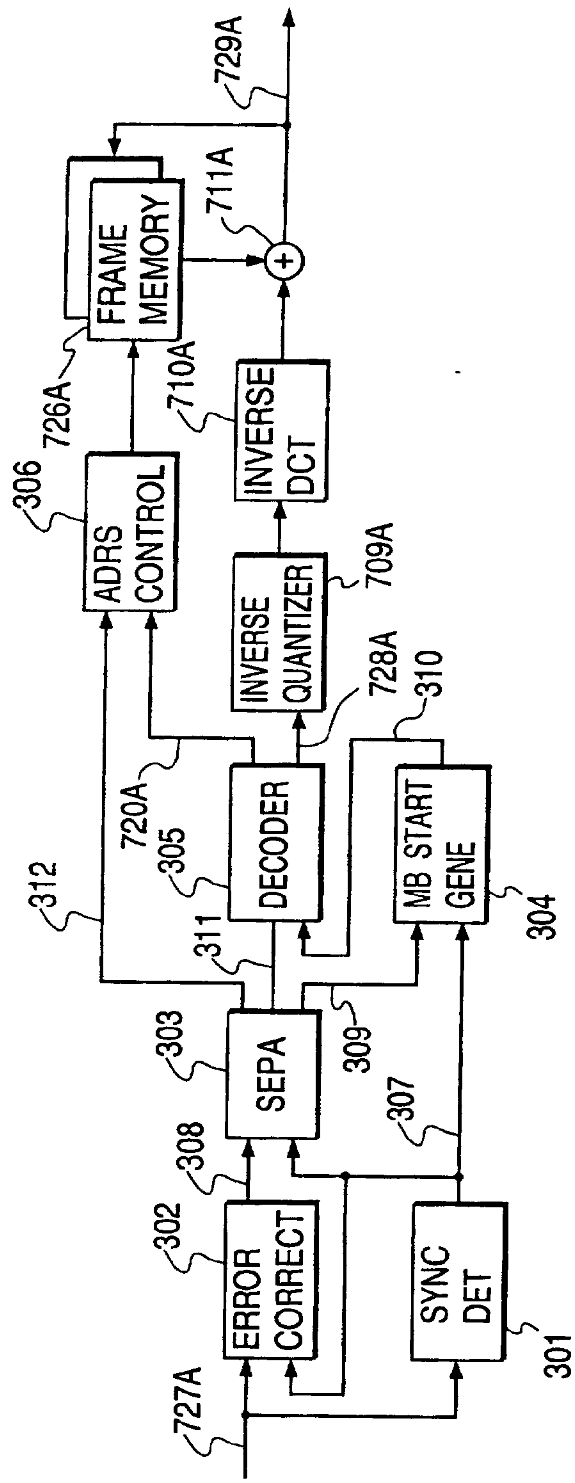

ERROR CORRECT
SYNC DET
SEPA
DECODER
MB START GENE
ADRS CONTROL
INVERSE QUANTIZER
INVERSE DCT
FRAME MEMORY
727A
301
302
303
304
305
306
307
308
309
310
311
312
709A
710A
711A
720A
726A
728A
729A

FIG. 6

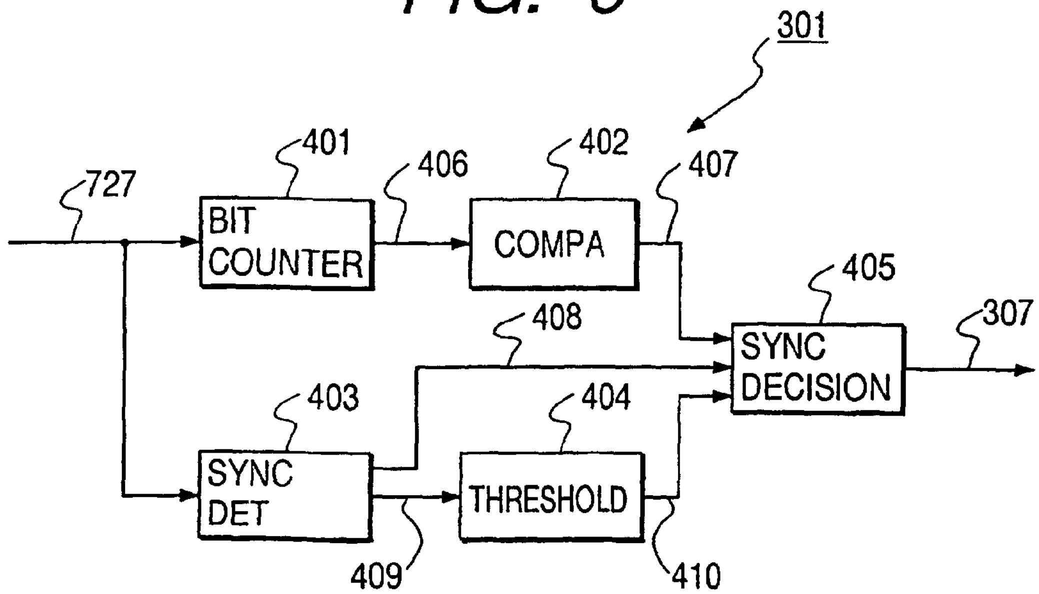

301
401
406
402
407
727
BIT COUNTER
COMPA
405
408
307
SYNC DECISION
403
404
SYNC DET
THRESHOLD
409
410

FIG. 7

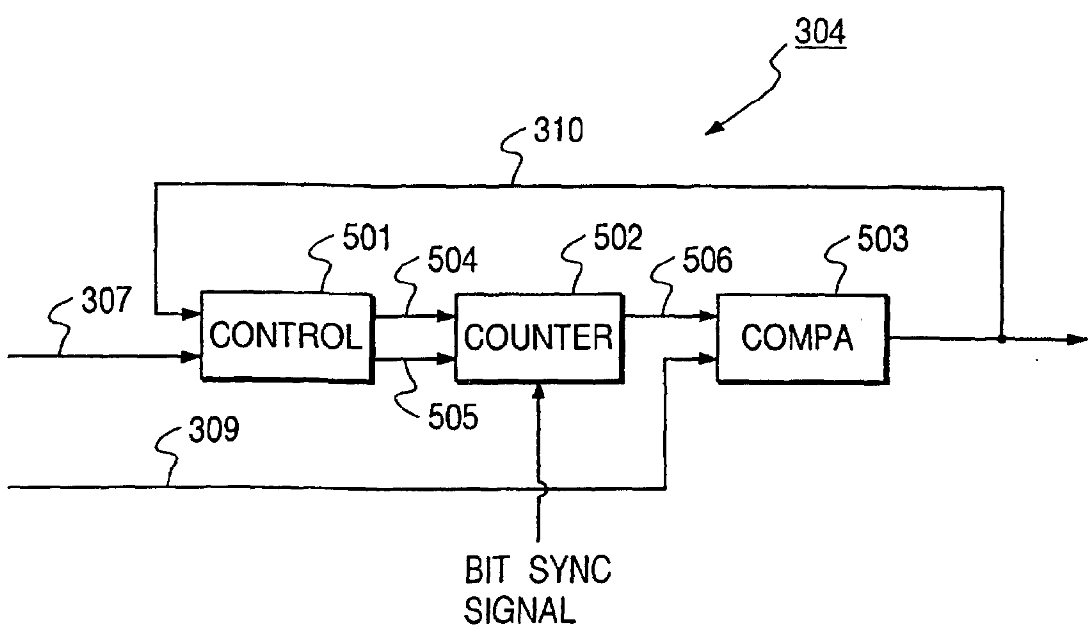
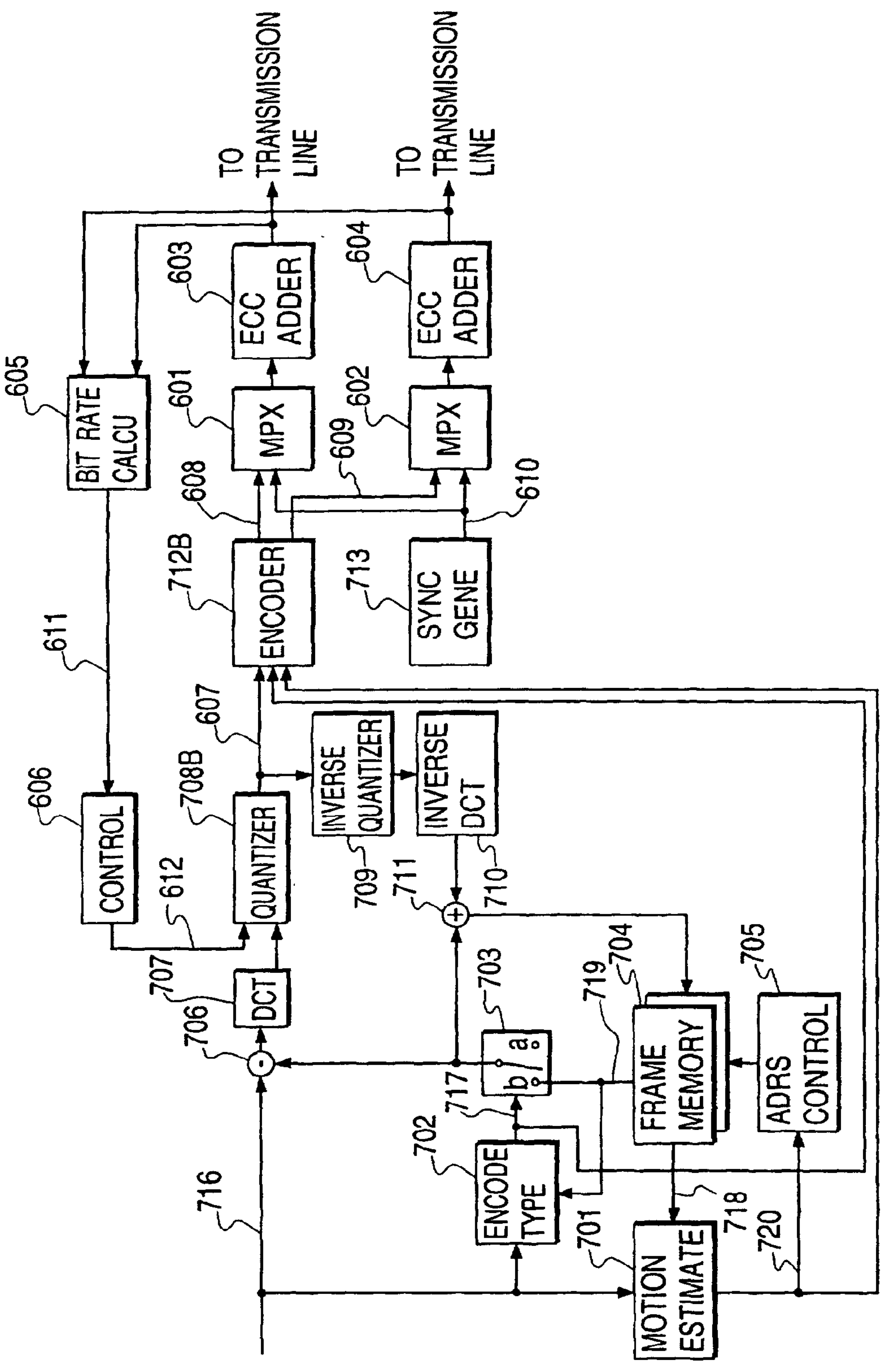

304
310
501
504
502
506
503
307
CONTROL
COUNTER
COMPA
505
309
BIT SYNC SIGNAL

FIG. 8


TO TRANSMISSION LINE
TO TRANSMISSION LINE
BIT RATE CALCU
ECC ADDER
ECC ADDER
MPX
MPX
ENCODER
SYNC GENE
CONTROL
QUANTIZER
INVERSE QUANTIZER
INVERSE DCT
DCT
FRAME MEMORY
ADRS CONTROL
ENCODE TYPE
MOTION ESTIMATE
b
a
605
603
604
601
602
608
609
610
611
712B
713
606
708B
607
612
707
706
709
711
710
703
704
719
705
702
717
716
701
718
720